Flip-Flop Basics

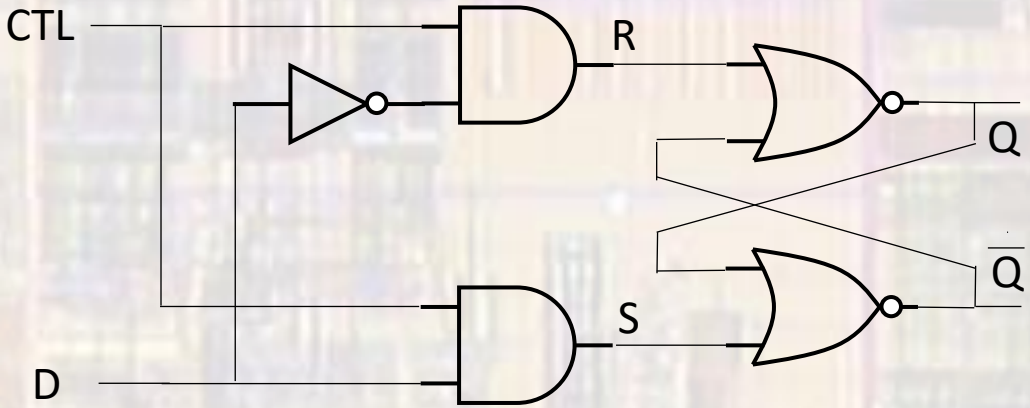
Last updated 1/11/21

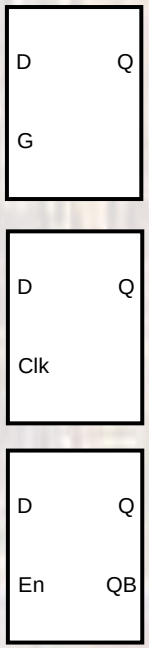
Flip-Flop Basics

- D Latch (data)

Level Sensitive Latch

CTL = low → latched
CTL = high → Transfer





CTL	D	Q
0	x	Q_{old}
1	D	D

Flip-Flop Basics

- D Flip-Flop (data)
  - Sequential
    - Bi-stable circuit
    - Synchronous – outputs change on a (rising) clk edge
    - Output changes limited to specific input conditions

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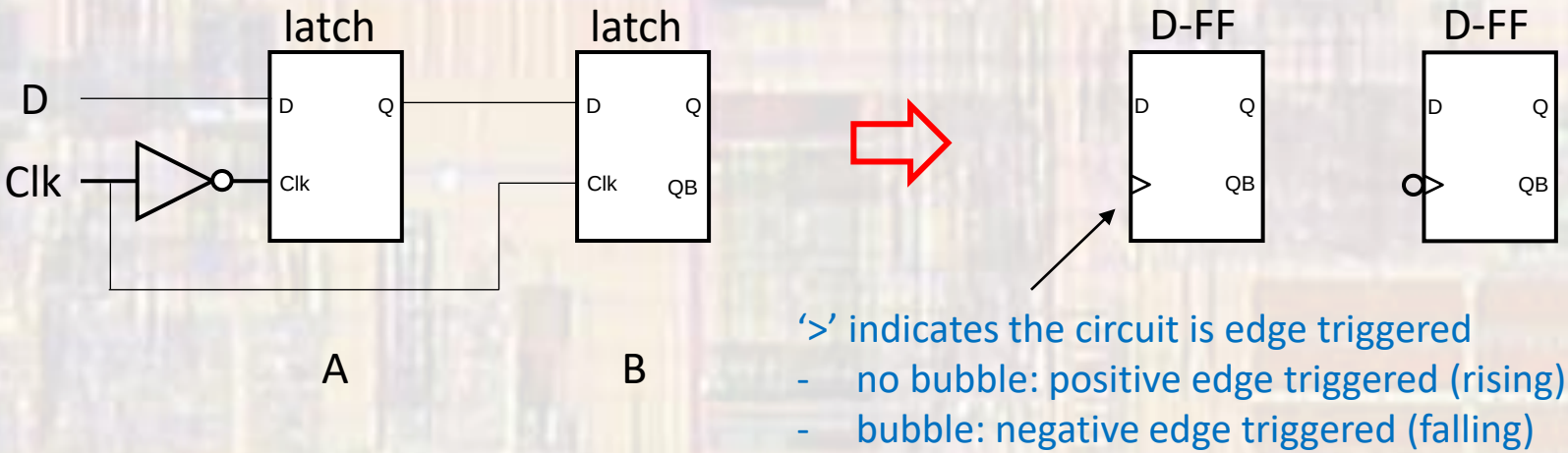
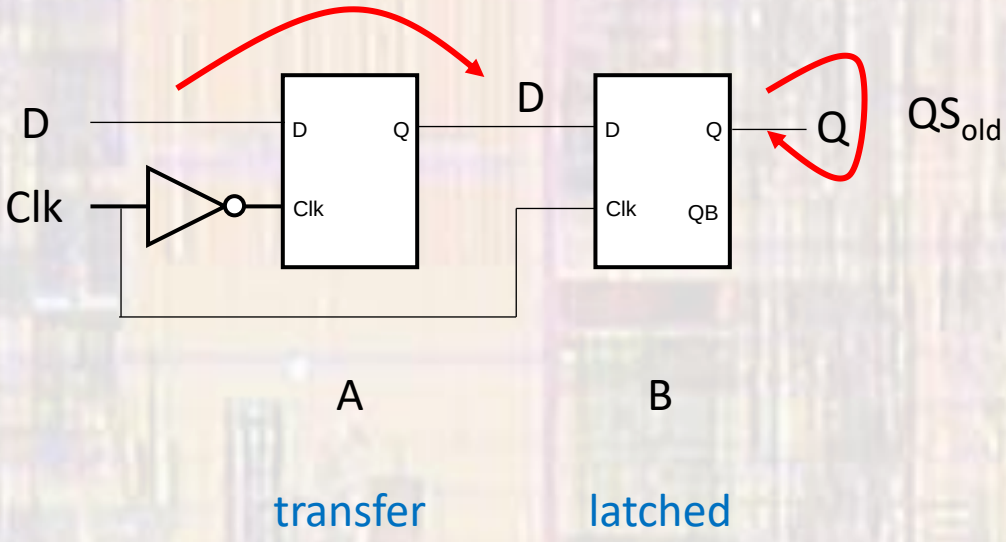


Flip-Flop Basics

D-Latch

CTL CLK	D	Q
0	x	Q_{old}
1	D	D

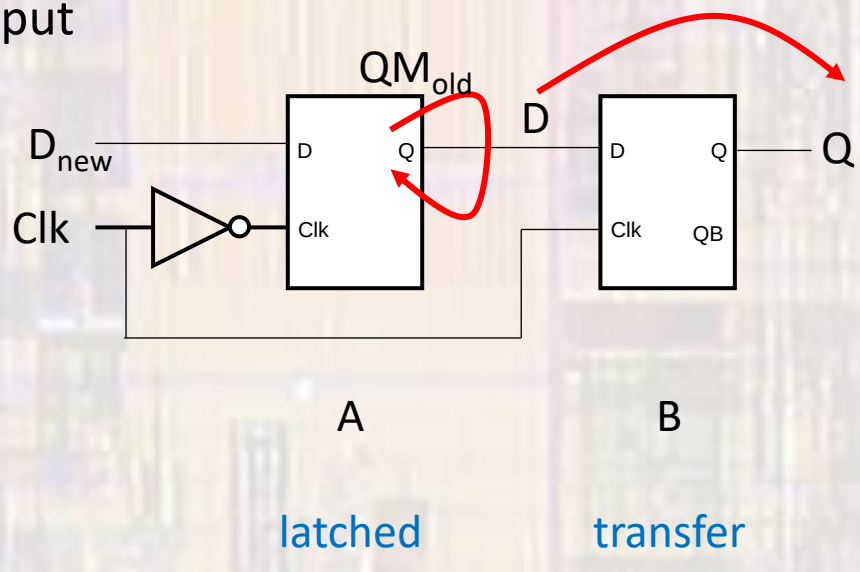
- D Flip-Flop (data)
  - Clock low – after a short time
    - A is enabled and passes D to it's Q output
    - B is in latch mode and retains it's state - QS_{old}



D	Clk	Q
x	0	QS_{old}

Flip-Flop Basics

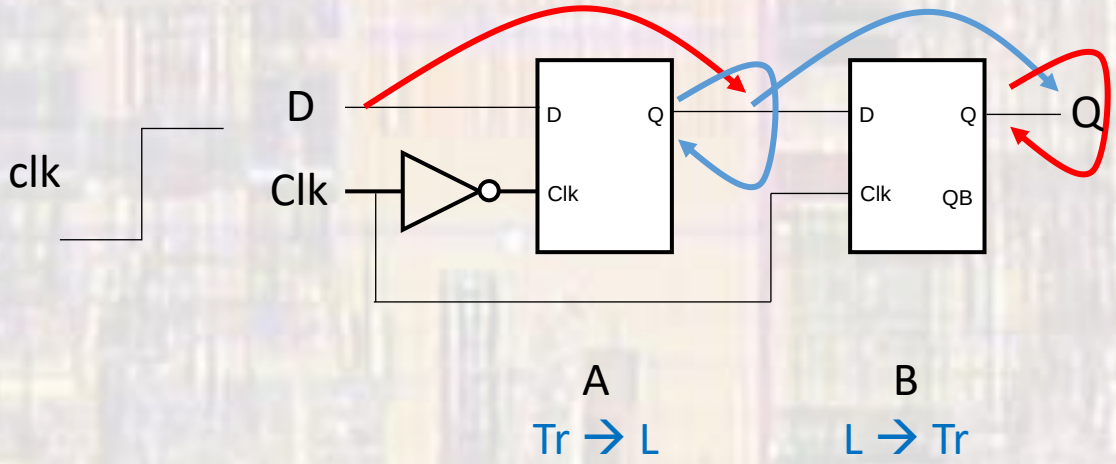
- D Flip-Flop (data)
  - Clock high – after a short time
    - A is latched and retains it's state – Qm_{old} (original value of D)
    - B is in transfer mode and would have already passed D to it's Q output



D	Clk	Q
x	0	Q_{old}
x	1	QM_{old} (D_{old})

Flip-Flop Basics

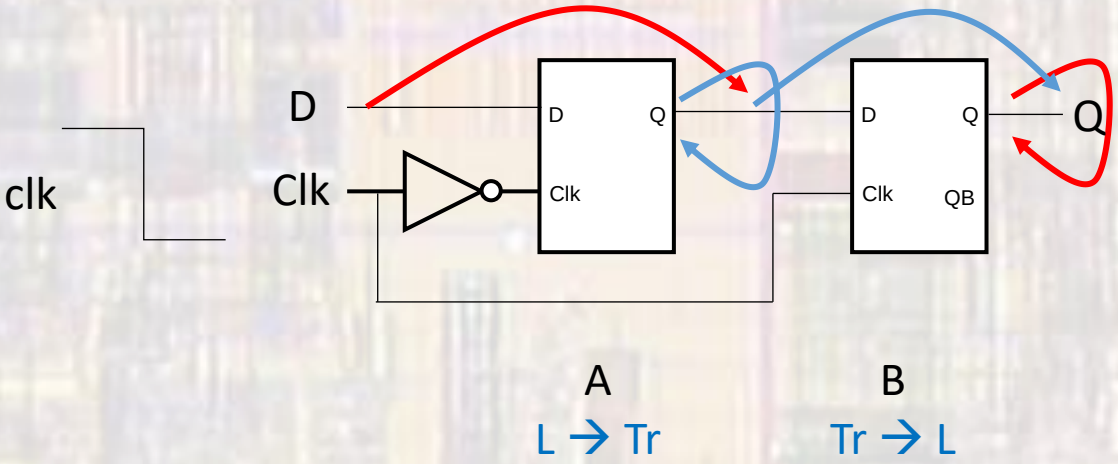
- D Flip-Flop (data)
  - Clock Low → High
    - D has previously been passed to the intermediate node
    - When clk transitions high, the intermediate value (D) is passed to the output while simultaneously the A becomes latched
    - Further changes of the D input are blocked by the latched A



D	Clk	Q
x	0	Q_{old}
x	1	QM_{old}
D	↑	D

Flip-Flop Basics

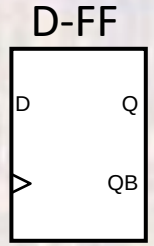
- D Flip-Flop (data)
  - Clock High → Low
    - The output is latched by the B
    - The new D input is allowed to transfer to the intermediate node but no further



D	Clk	Q
x	0	Q_{old}
x	1	QM_{old}
D	↑	D
x	↓	QM_{old}

Flip-Flop Basics

- D Flip-Flop (data)
  - Truth Table
    - Positive Edge Triggered D Flip-Flop
      - (typically, just called a D Flip-flop)



D	Clk	Q
x	0	Q_{old}
x	1	Q_{old}
D	↑	D
x	↓	Q_{old}