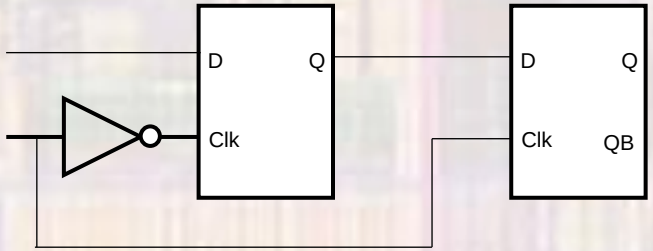
Flip-Flop Enhancements

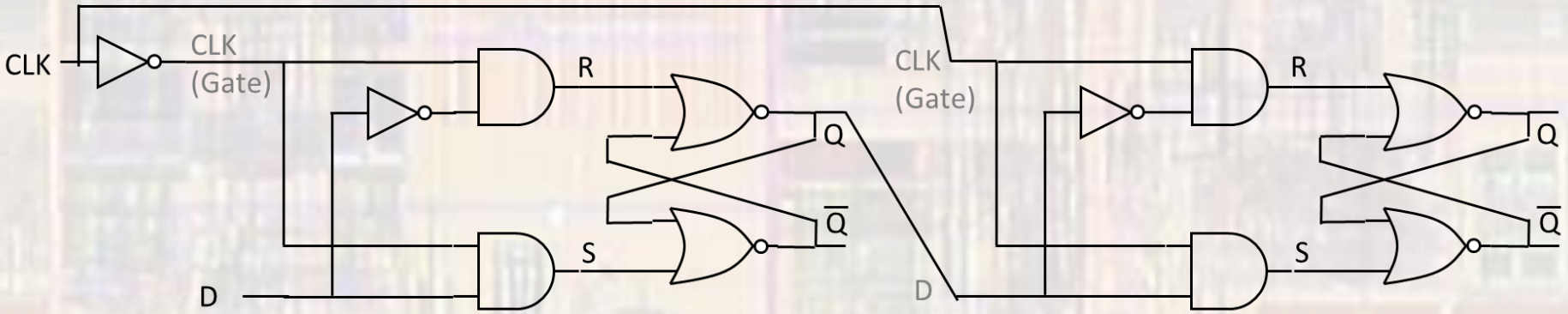
Last updated 1/11/21

Flip-Flop Enhancements

- D Flip-Flop – SR Latch based



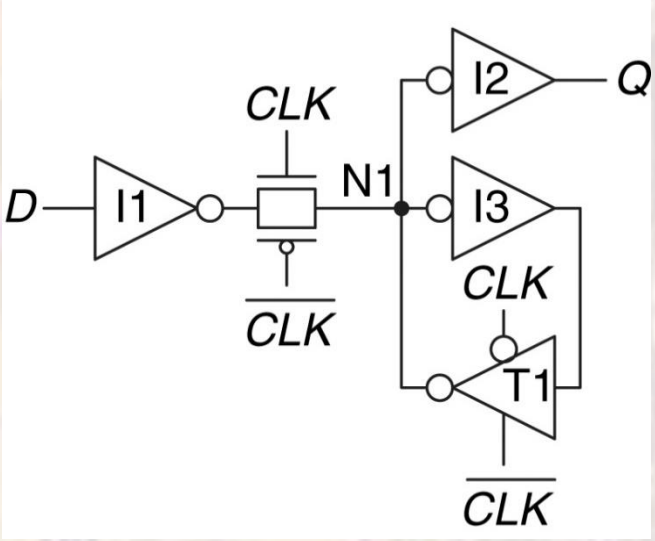
master slave



How many Transistors ???

Flip-Flop Enhancements

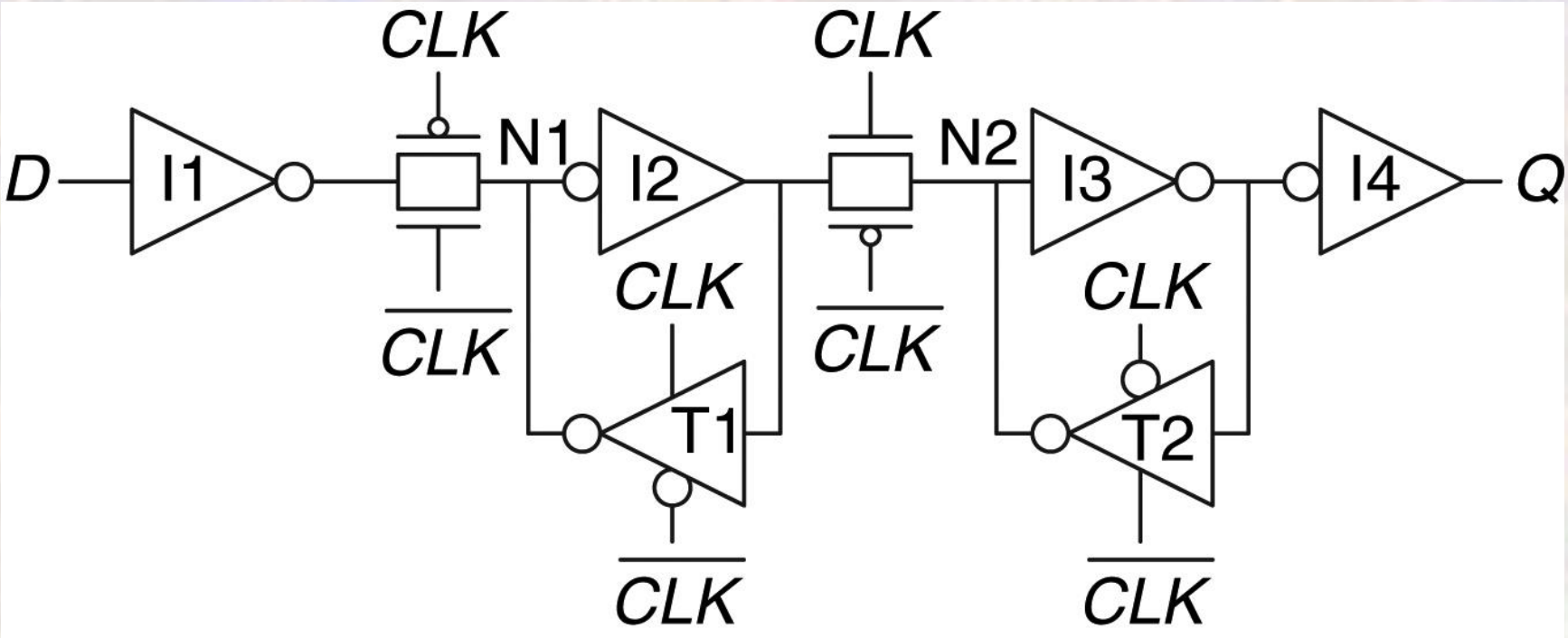
- D Flip-Flop – Pass Gate based
  - D latch



src: Harris & Harris

Flip-Flop Enhancements

- D Flip-Flop – Pass Gate Based



src: Harris & Harris

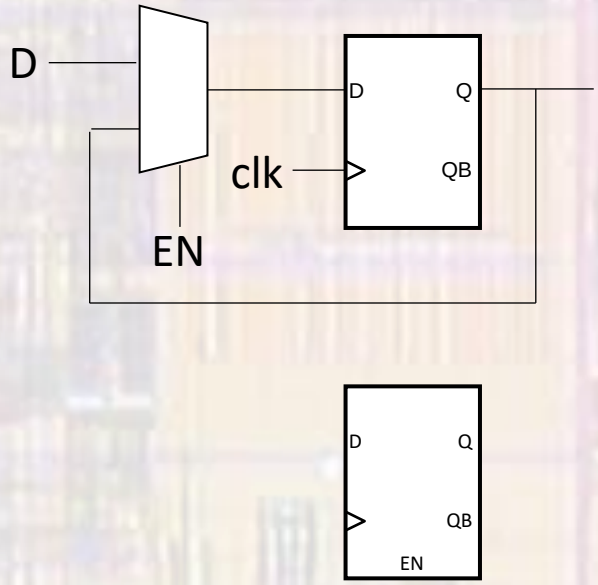
How many Gates ???

Flip-Flop Enhancements

- Enhanced D Flip-Flops
  - Enable – limit when the FF responds to the clk
  - Set – force the FF into the Q=1 state, independent of D
  - Reset – force the FF into the Q=0 state, independent of D
  - Set/Reset can be asynchronous or synchronous
  - Enable/Set/Reset – can be active high or active low

Flip-Flop Enhancements

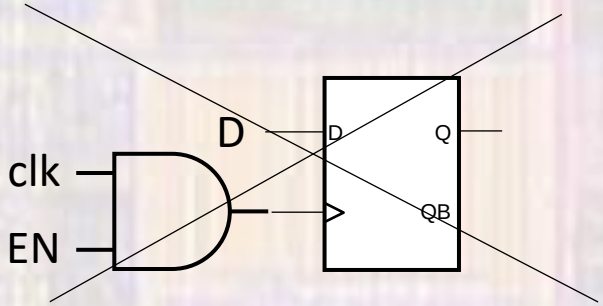
- Enhanced D Flip-Flops
  - Synchronous Enable - mux



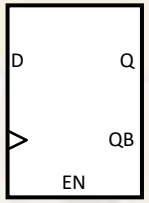
D	Clk	EN	Q
x	x	0	Q_{old}
x	0	1	Q_{old}
x	1	1	Q_{old}
x	↓	1	Q_{old}
D	↑	1	D

Flip-Flop Enhancements

- Enhanced D Flip-Flops
  - Synchronous Enable – gated clock



Requires EN only changes when clk is low

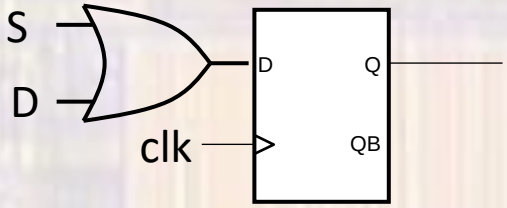


D	Clk	EN	Q
x	x	0	Q_{old}
x	0	1	Q_{old}
x	1	1	Q_{old}
x	↓	1	Q_{old}
D	↑	1	D

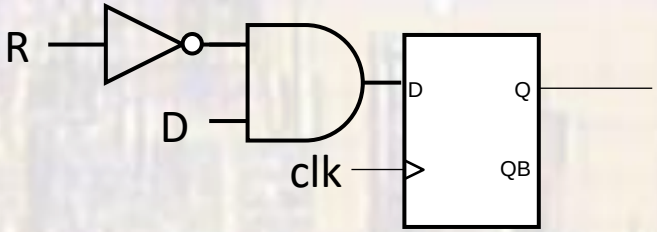
Normally clock gating is considered bad practice at the system level

Flip-Flop Enhancements

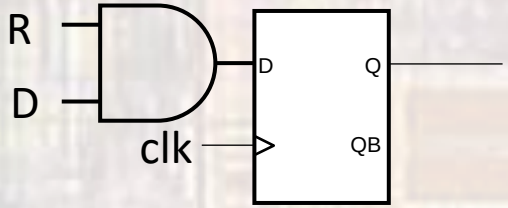
- Enhanced D Flip-Flops
  - Synchronous Set



  - Synchronous Reset - RST

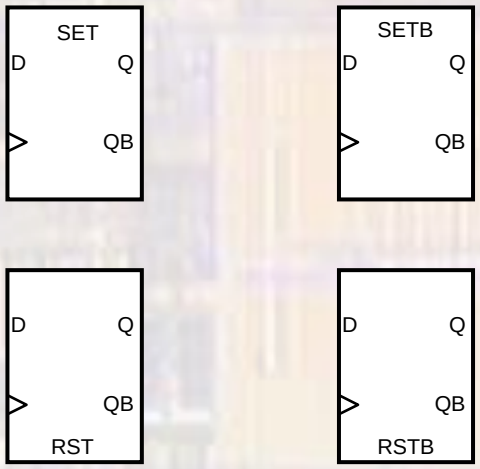


Reset_bar – RSTB



Flip-Flop Enhancements

- Enhanced D Flip-Flops
  - Synchronous Set/Reset – very uncommon

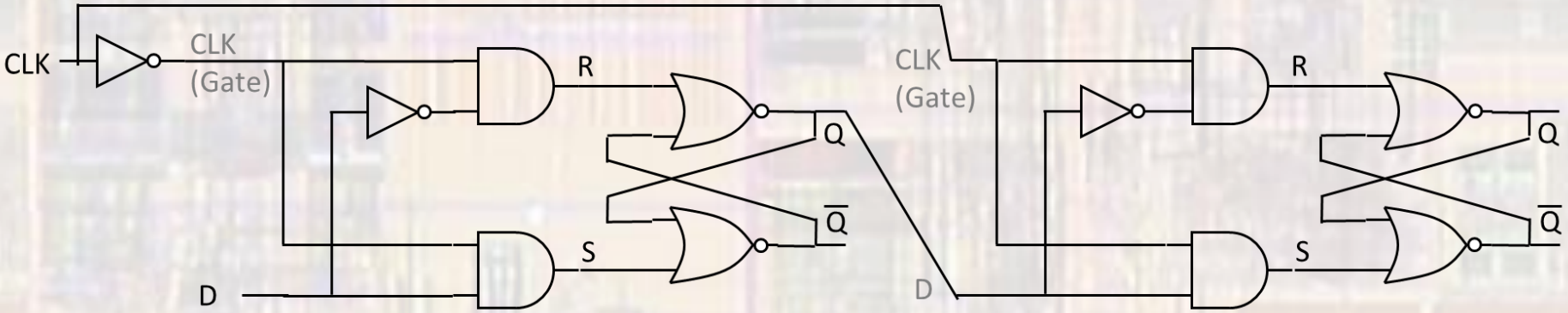


D	Clk	SET	RST	Q
x	0	x	x	Q_{old}
x	1	x	x	Q_{old}
x	↓	x	x	Q_{old}
D	↑	0	0	D
x	↑	1	-	1
x	↑	-	1	0

SETB / RSTB operate in active low mode

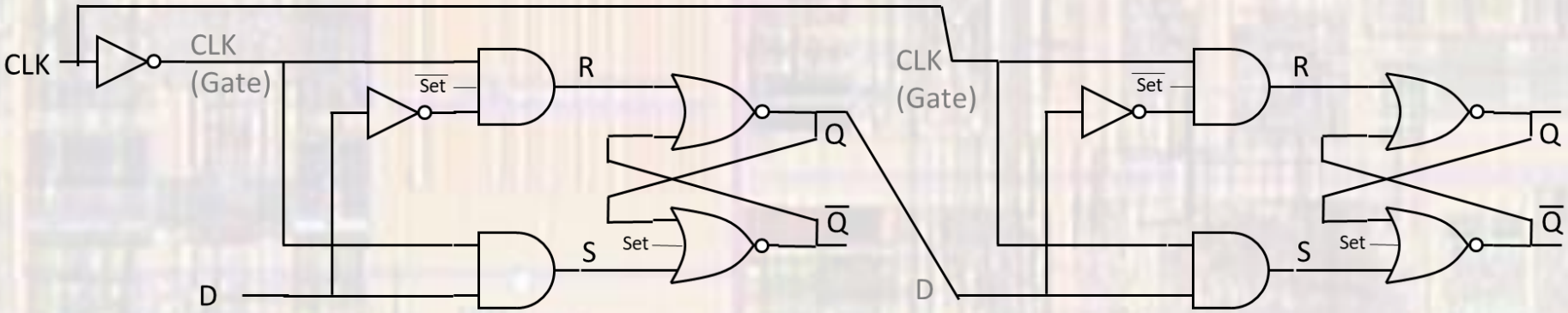
Flip-Flop Enhancements

- Enhanced D Flip-Flops
  - Asynchronous Set/Reset
    - Due to the latching behavior of the DFF – require internal circuit changes



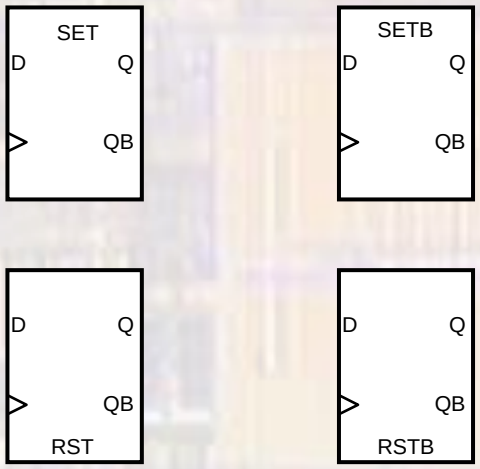
Flip-Flop Enhancements

- Enhanced D Flip-Flops
  - Asynchronous Set
    - Due to the latching behavior of the DFF – require internal circuit changes



Flip-Flop Enhancements

- Enhanced D Flip-Flops
  - Asynchronous Set/Reset

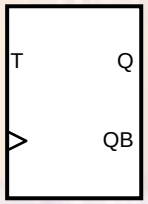


D	Clk	SET	RST	Q
x	0	0	0	Q_{old}
x	1	0	0	Q_{old}
x	↓	0	0	Q_{old}
D	↑	0	0	D
x	x	1	-	1
x	x	-	1	0

SETB / RSTB operate in active low mode

Flip-Flop Enhancements

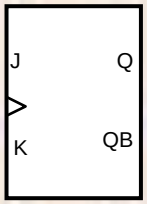
- Additional Flip-Flops
  - T – Flip-Flop (Toggle)



T	Clk	Q
x	0	Q_{old}
x	1	Q_{old}
x	↓	Q_{old}
0	↑	Q_{old}
1	↑	$\overline{Q_{old}}$

Flip-Flop Enhancements

- Additional Flip-Flops
  - JK – Flip-Flop



J	K	clk	Q
x	x	0	Q_{old}
x	x	1	Q_{old}
x	x	↓	Q_{old}
0	0	↑	Q_{old}
0	1	↑	0
1	0	↑	1
1	1	↑	$\overline{Q_{old}}$

Matches the J input