Flip-Flop Timing

Last updated 1/11/21
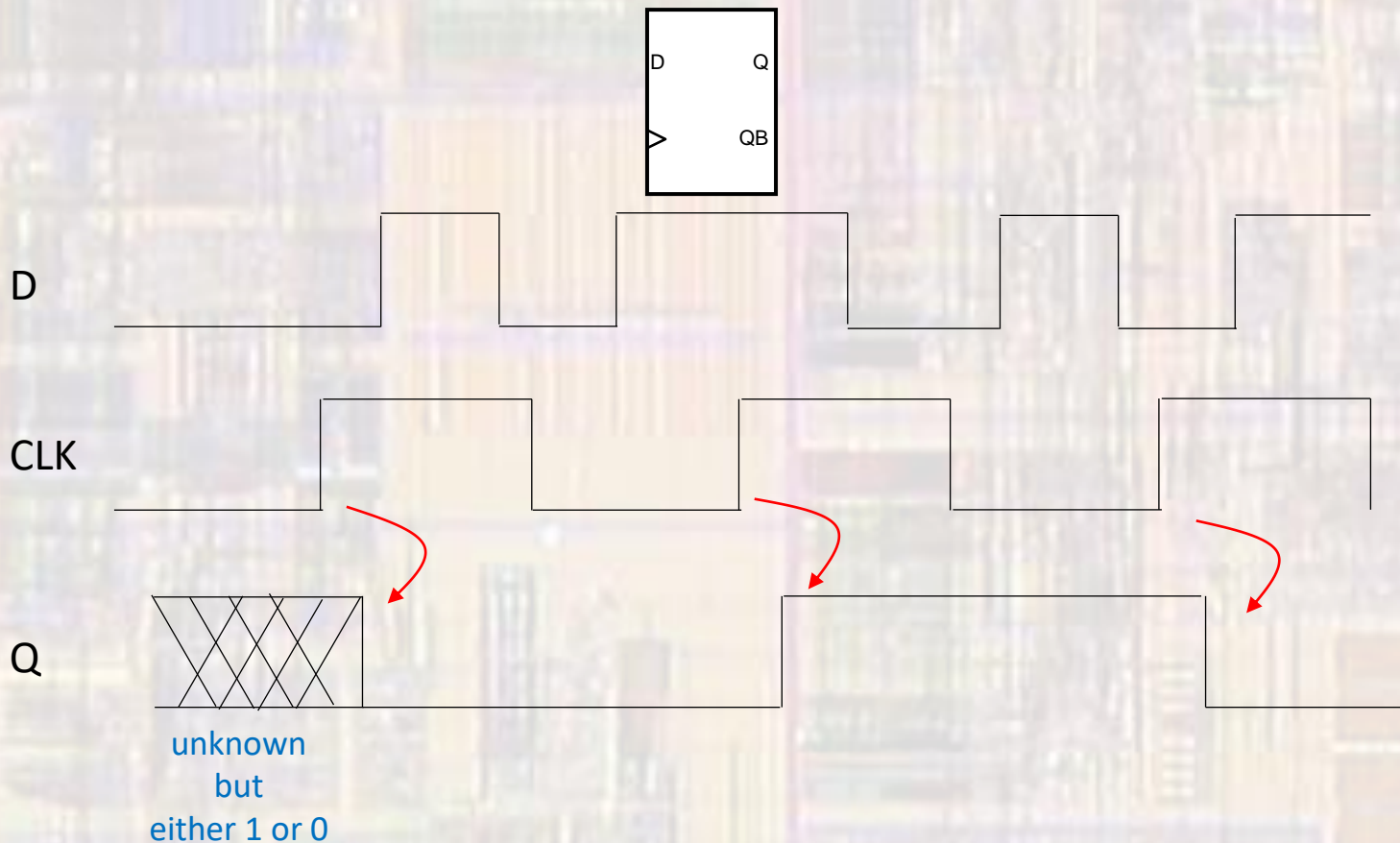
Flip-Flop Timing

- D Flip-Flop (data)
  - Edge triggered
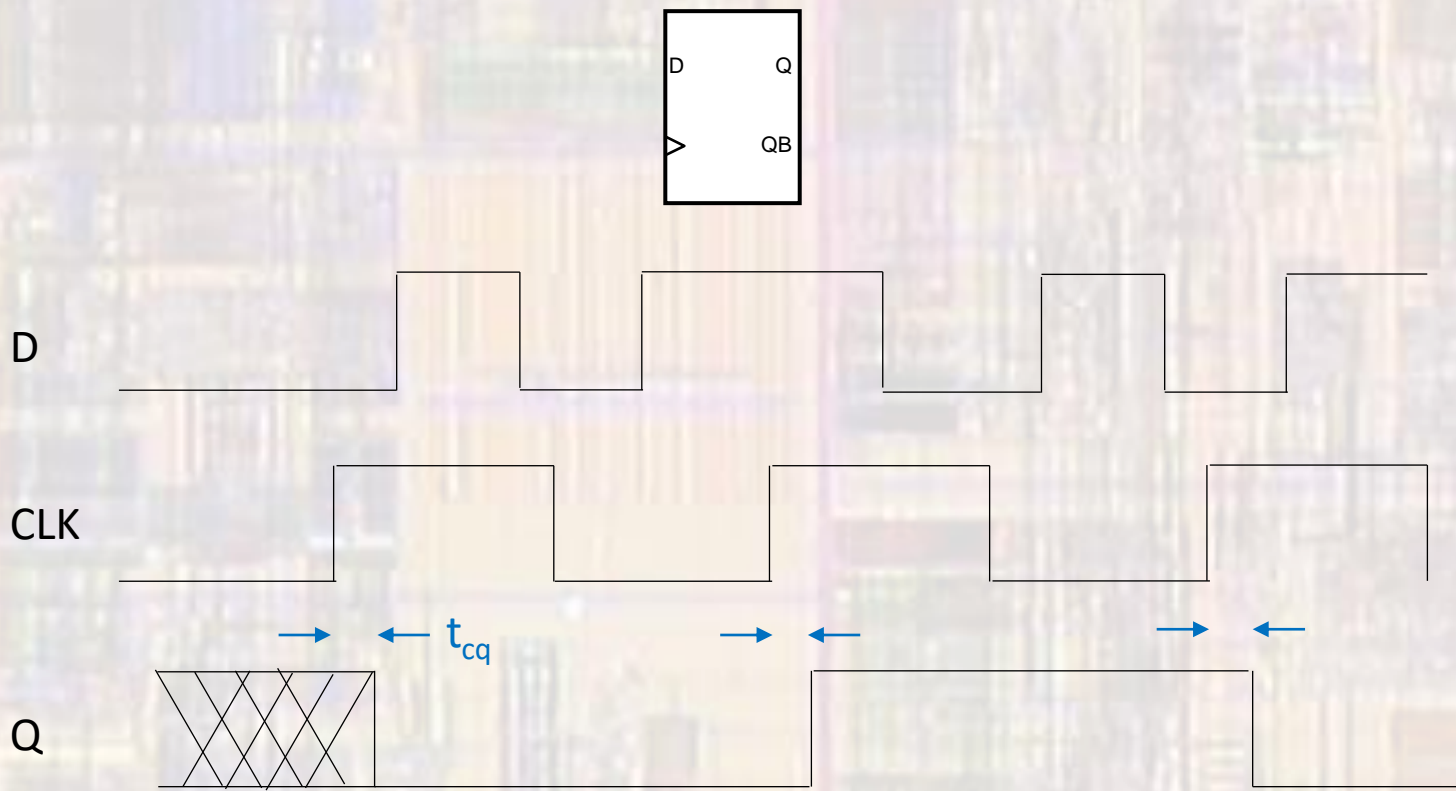

nothing happens

D

CLK

rising edge triggered
something 'can' happen
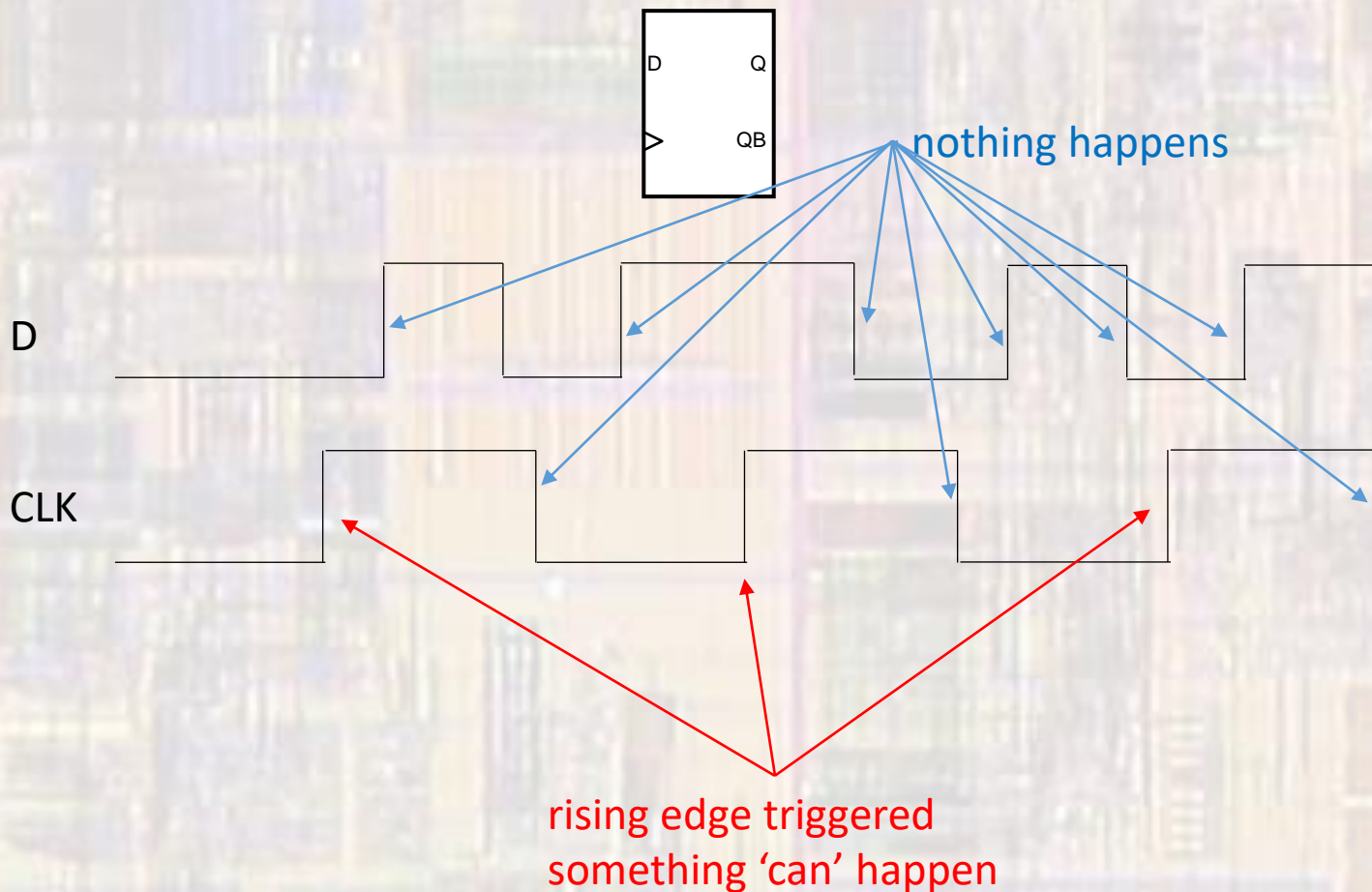
Flip-Flop Timing

- D Flip-Flop (data)
  - Edge triggered
  - Delay from clk to output change
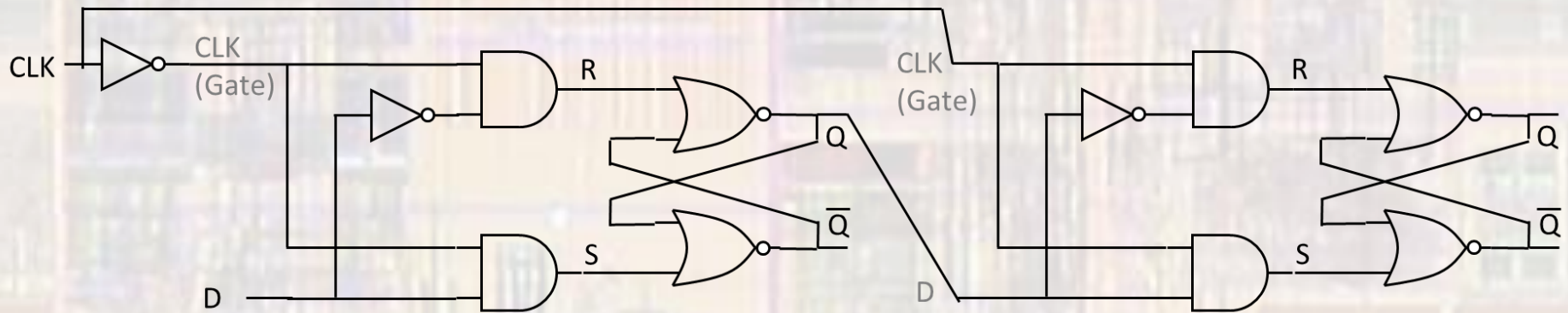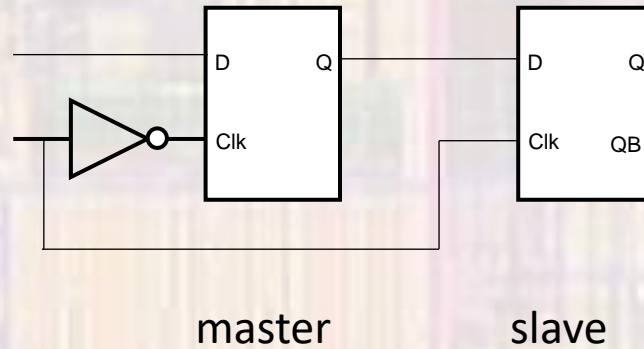

unknown
but
either 1 or 0

Flip-Flop Timing

- D Flip-Flop (data)
  - t_{cq} – time from clk to Q valid

Flip-Flop Timing

- D Flip-Flop – T_{CQ}

- D Flip-Flop - T_{CQ}

- D Flip-Flop - T_{CQ}

master   slave

clk low – DC state

transfer   latched

Flip-Flop Timing

- D Flip-Flop - T_{CQ}

t = 0 at clock edge

master   slave

- D Flip-Flop - T_{CQ}

Flip-Flop Timing

- D Flip-Flop - T_{CQ}

After 1.5 ns

master   slave
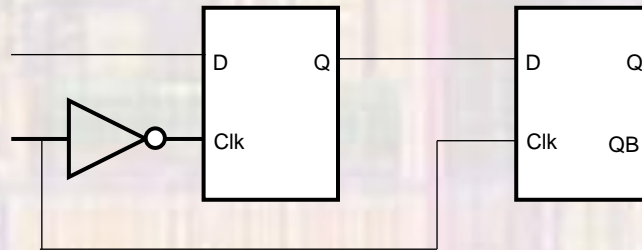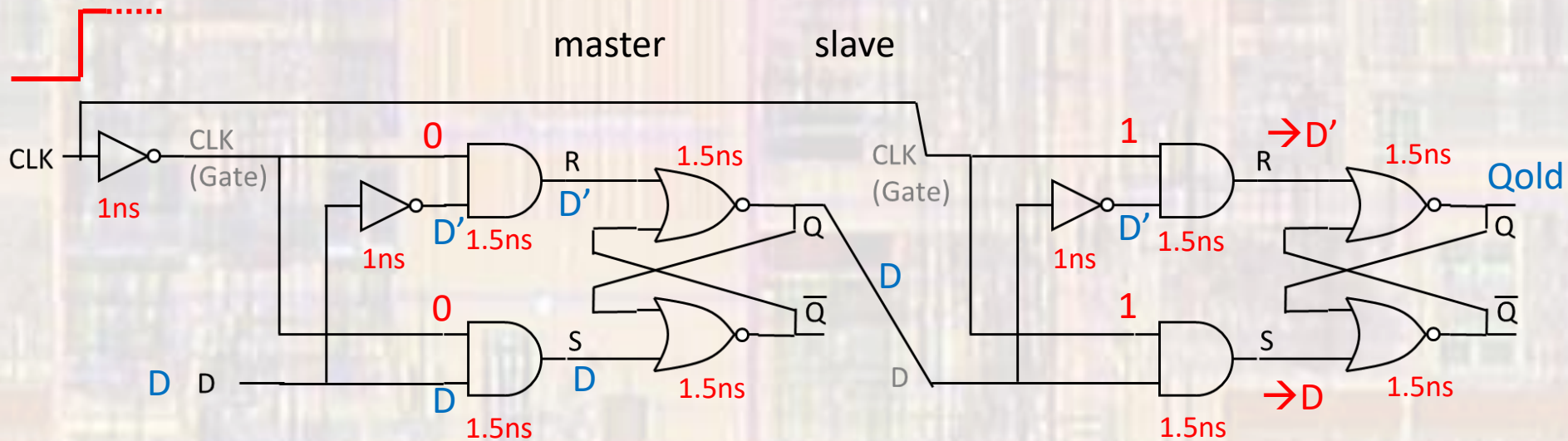
Flip-Flop Timing
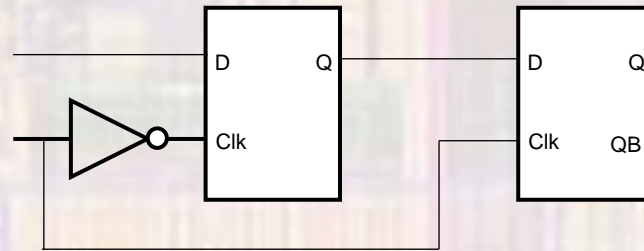
- D Flip-Flop - T_{CQ}

After 2.5 ns

master slave

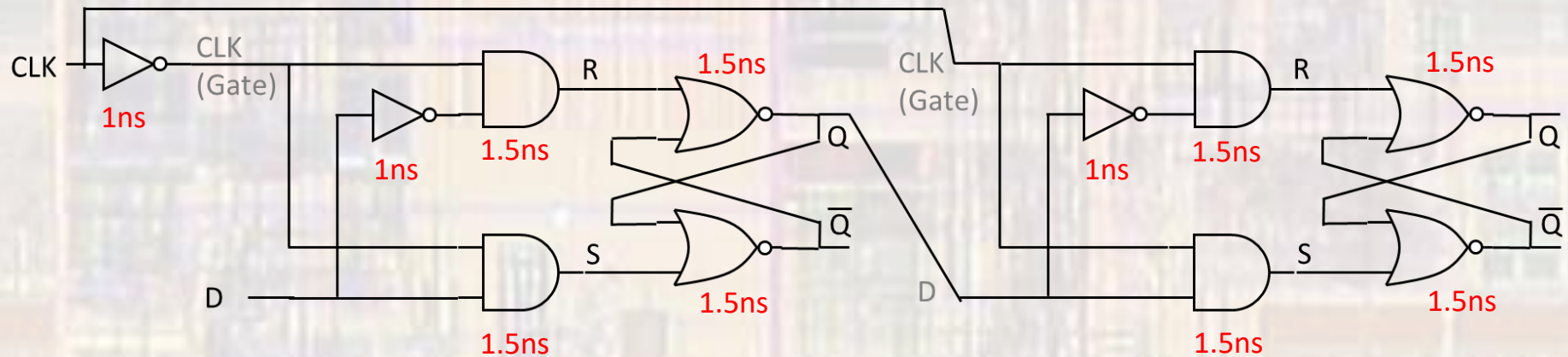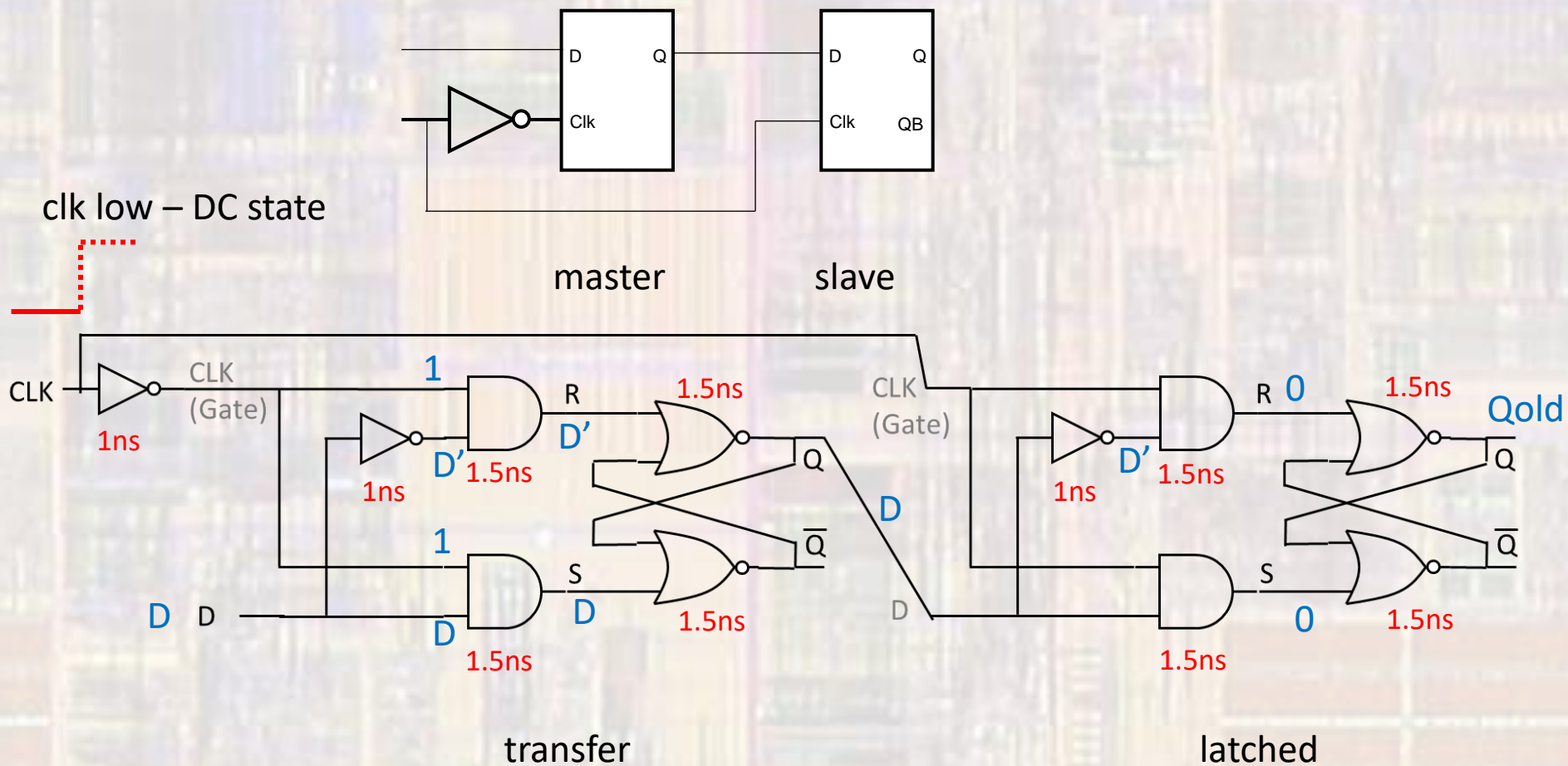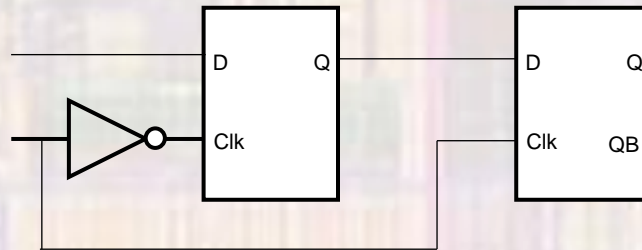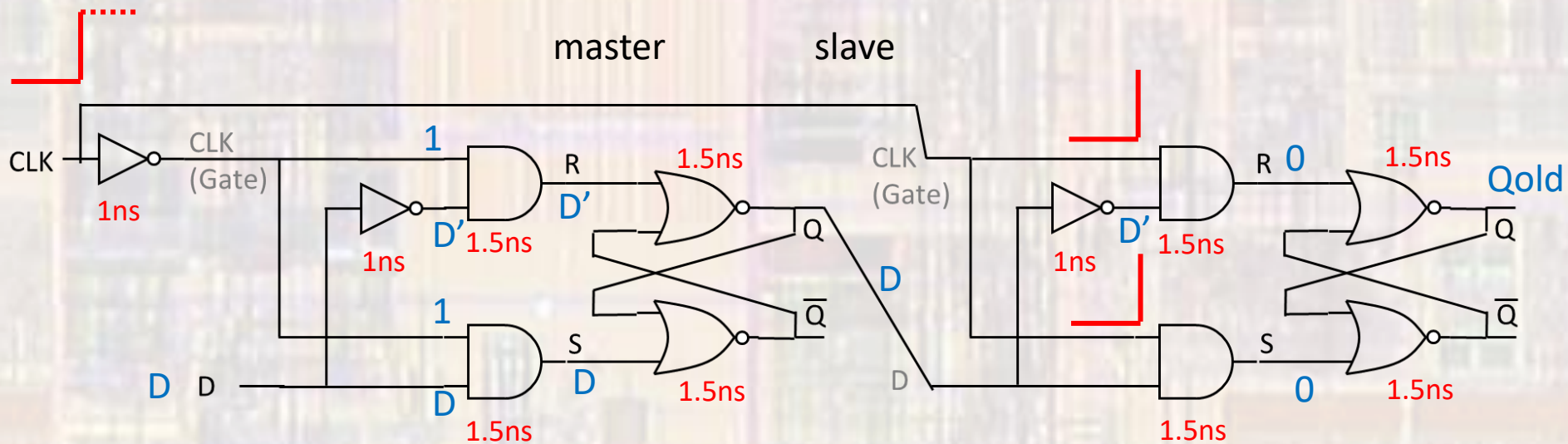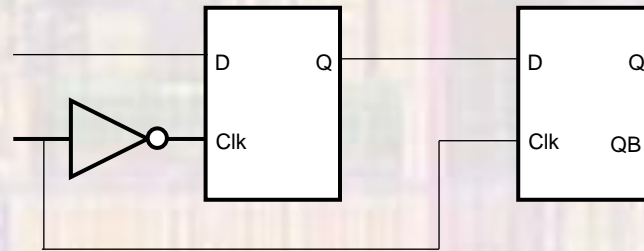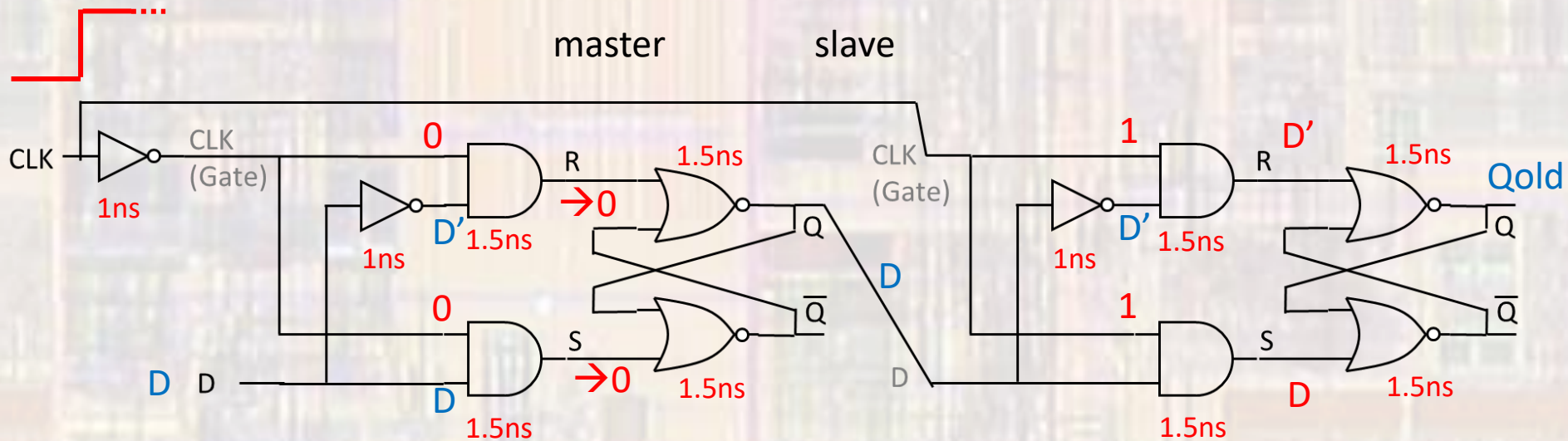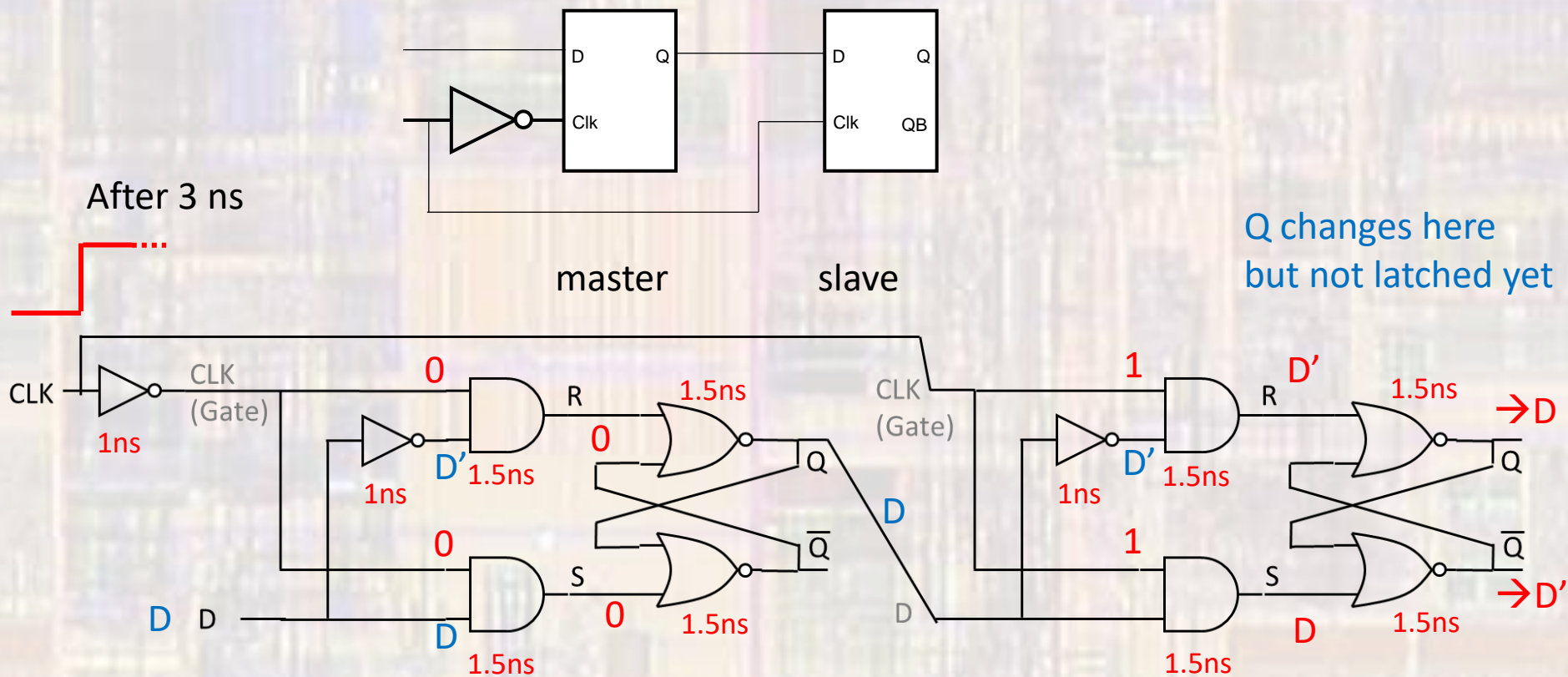# Flip-Flop Timing

- D Flip-Flop - T_{CQ}

Flip-Flop Timing
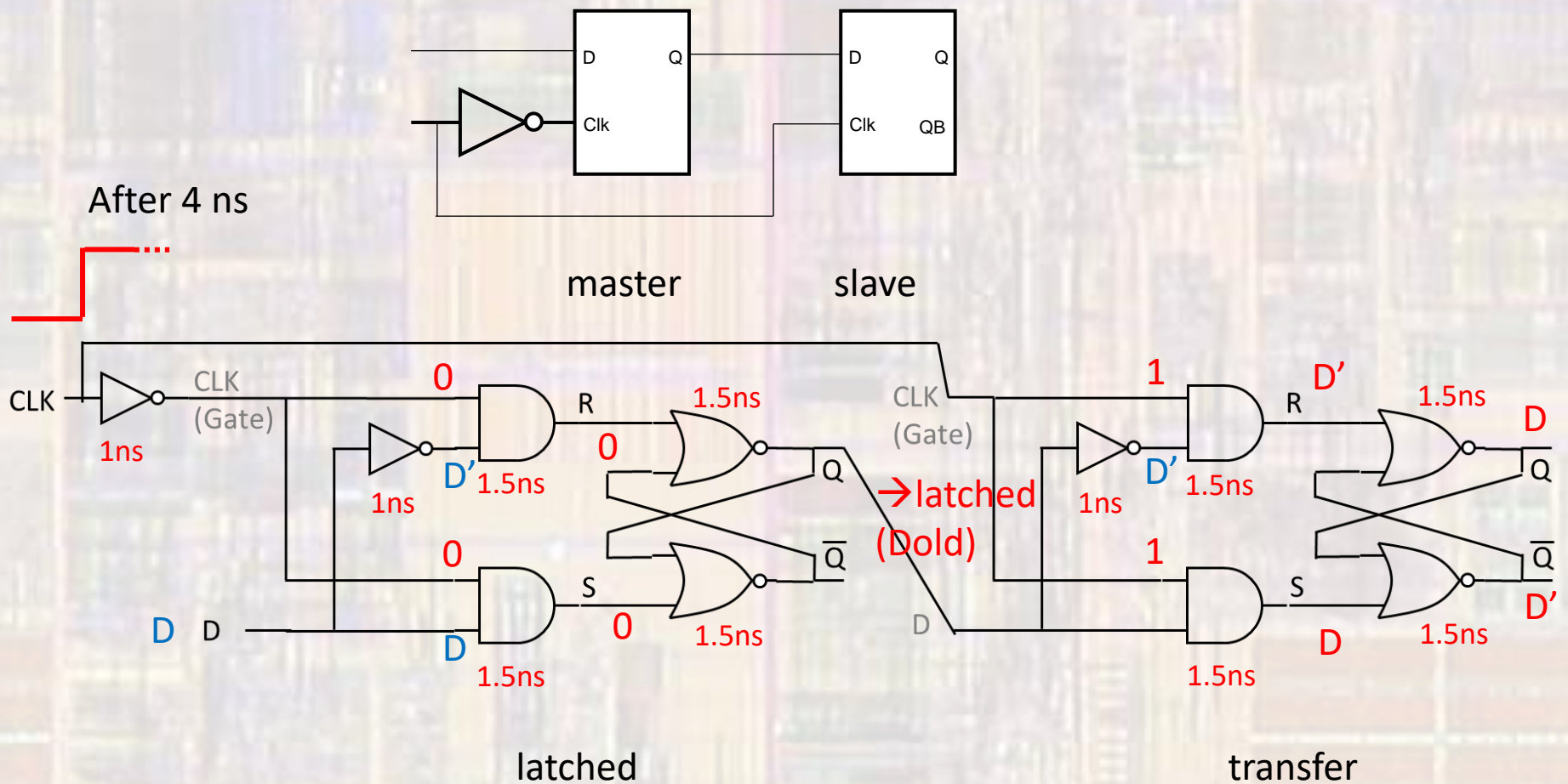
- D Flip-Flop - T_{CQ}

- D Flip-Flop - T_{CQ}

After 4.5 ns

master   slave

Q_M is latched now
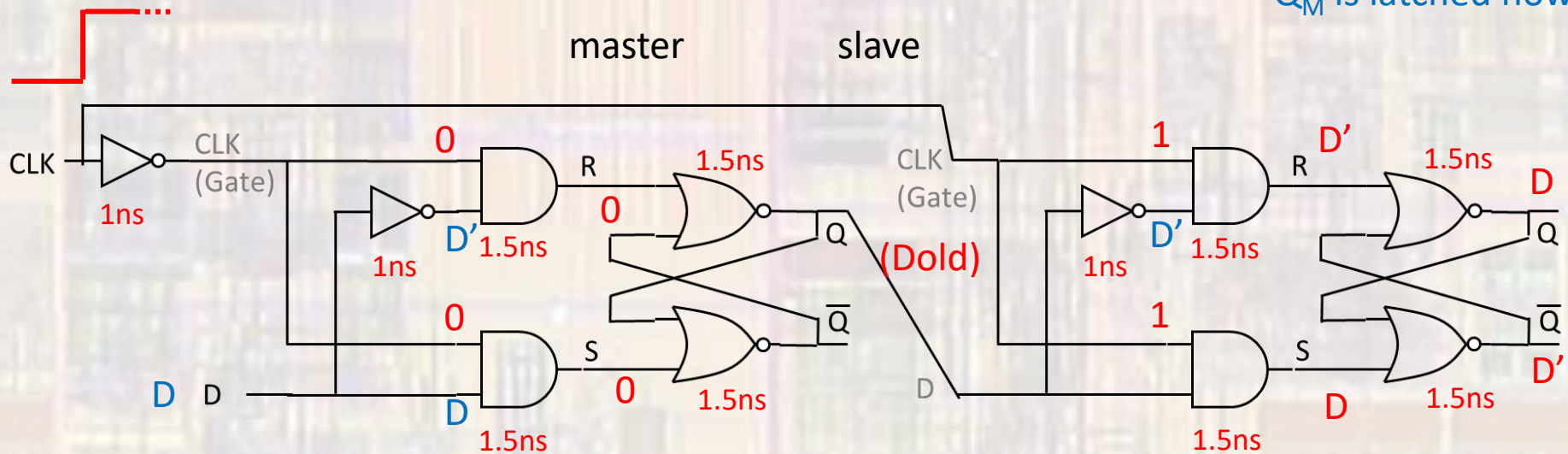
Flip-Flop Timing

- D Flip-Flop – T_{SU}
  - Time D must be stable before the clock edge
  - Not as bad as this would indicate (more analysis required)
    - Typically, T_{SU} is small compared to T_{CQ}

clk low – DC state

We assumed D was stable here

It takes 4.5ns for D to be stable if we changed it → T_{SU} = 4.5ns
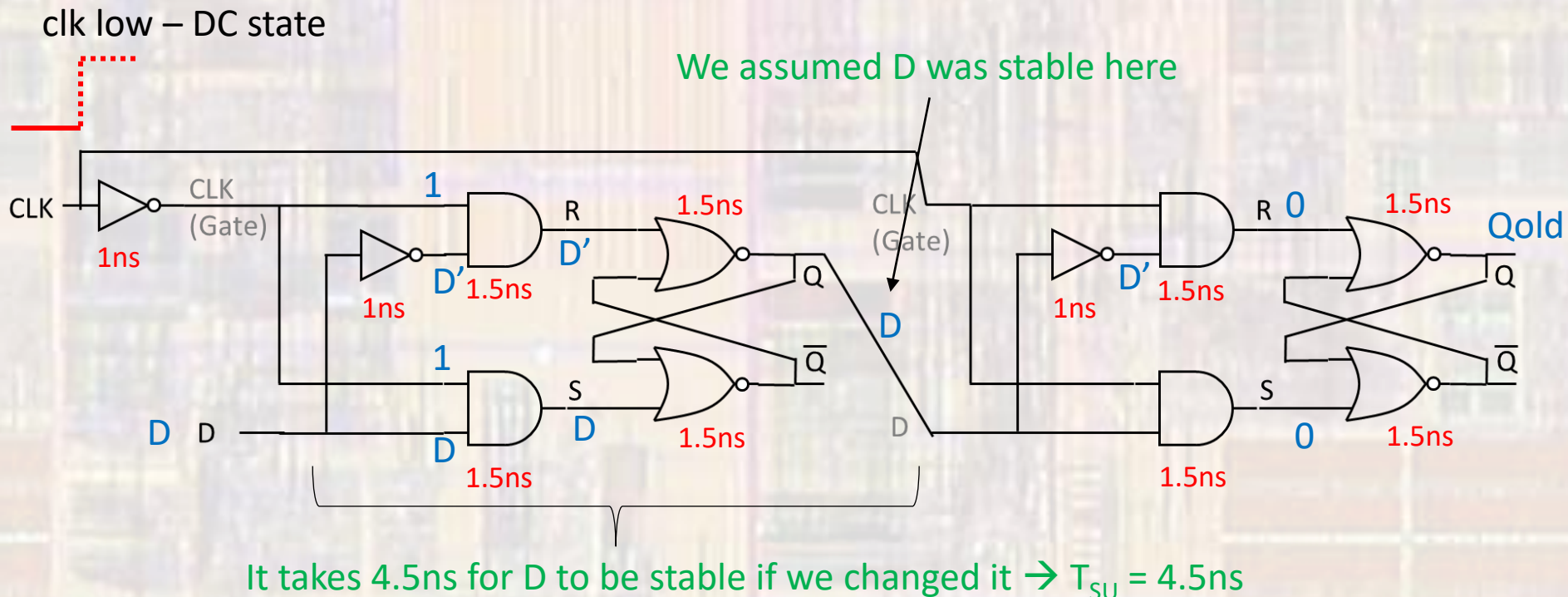
Flip-Flop Timing

- D Flip-Flop – T_{HOLD}
  - Time D must remain stable after the clock edge
  - Not as bad as this would indicate (more analysis required)
    - Typically, T_{HOLD} is designed to be 0ns

After 4 ns

The master is not latched until 4ns → T_{HOLD}

Flip-Flop Timing

- D Flip-Flop – T_{CQ}

SET
D
Q
QB
RSTB

CLK · CLK · N1 · I2 · CLK · N2 · I3 · I4 · Q

D — I1

$\overline{CLK}$ · T1 · $\overline{CLK}$ · T2 · $\overline{CLK}$

No RSTB or SET shown
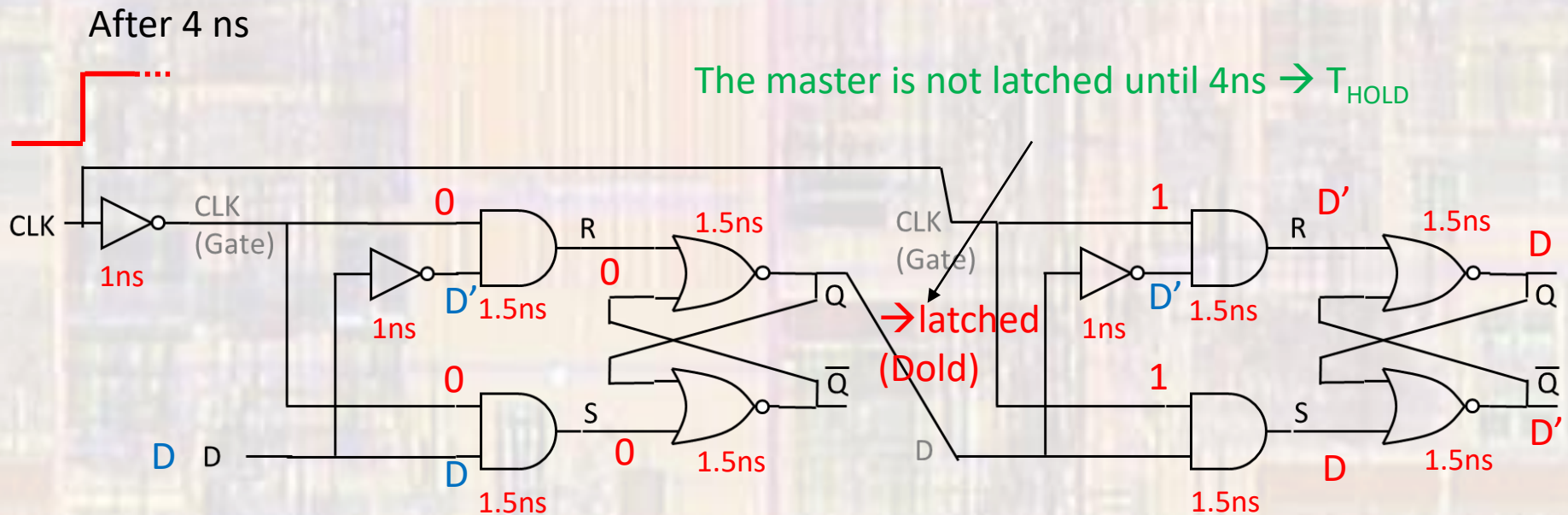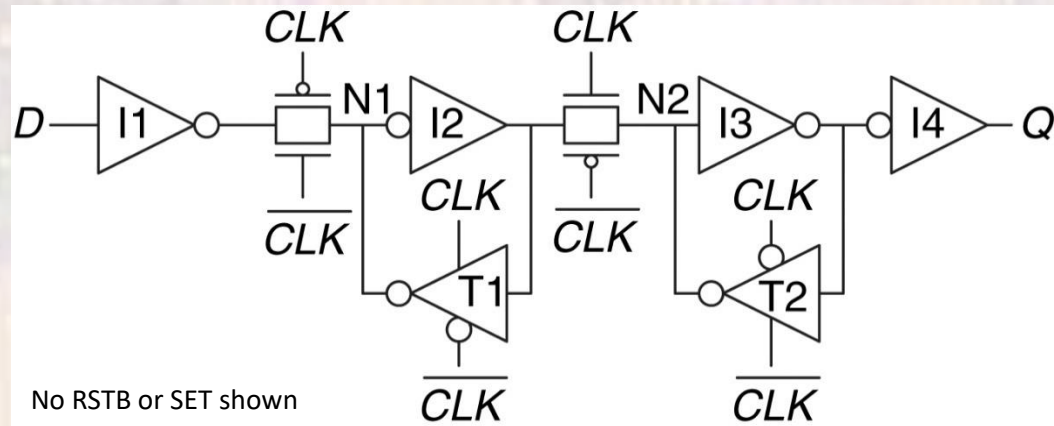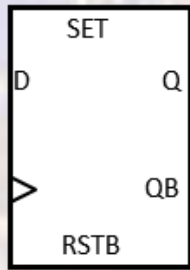
- Propagation Delays
  - Clk to Q
  - Clk to QB
  - RSTB to Q
  - SET to Q
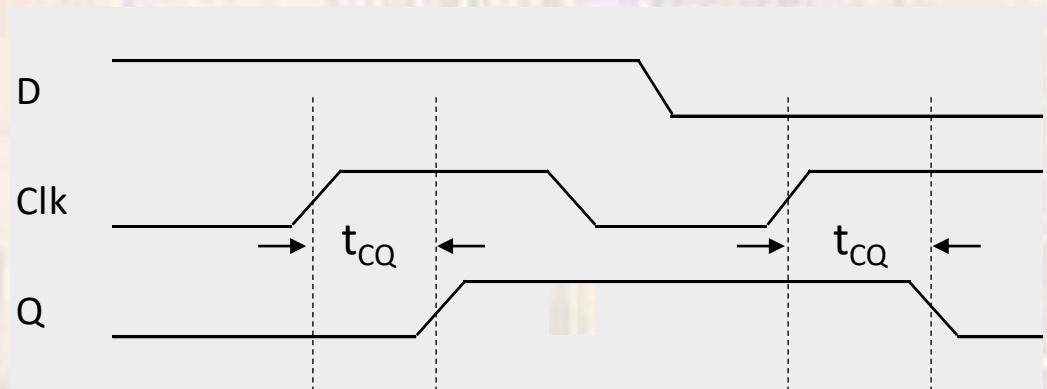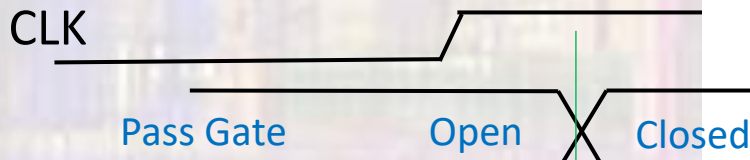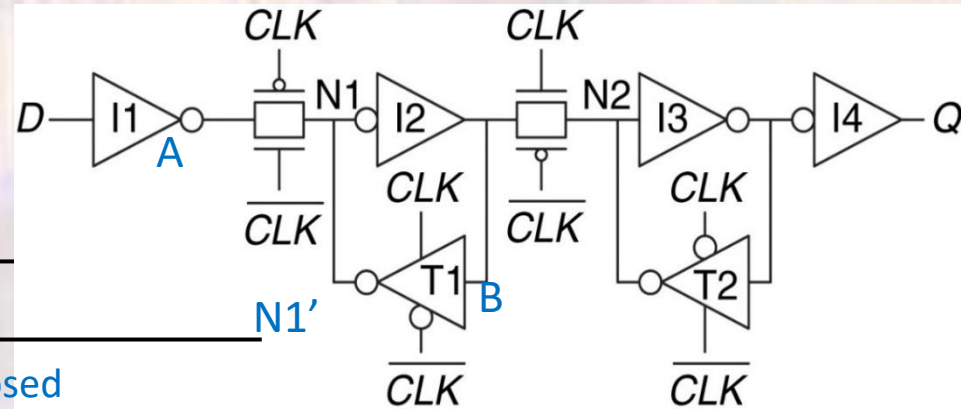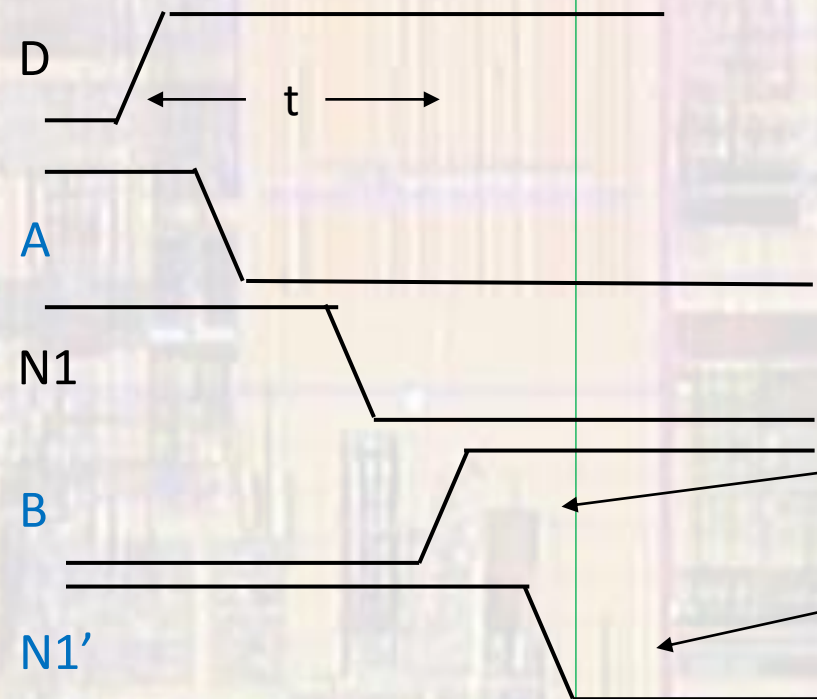
  ...

D

Clk

t_{CQ}

t_{CQ}

Q

Flip-Flop Timing

- ## D Flip-Flop – T_{SU}
  - ### Data changes before Clk ↑

CLK

Pass Gate   Open   Closed

D

t

case 1

A

N1

B

N1'

Proper operation requires the data to be stable for some amount of time before the clock rises → SETUP TIME

Input is ready for second latch

Input is supported by feedback

(circuit diagram labels) CLK, CLK, D, I1, A, N1, I2, $\overline{CLK}$, N1', T1, B, $\overline{CLK}$, CLK, CLK, N2, I3, I4, Q, CLK, T2, $\overline{CLK}$

Flip-Flop Timing

- ## D Flip-Flop – T_{SU}
  - ### Data changes before Clk ↑

CLK

Pass Gate   Open   Closed

N1'

D

← t →

case 2

A

N1

B

N1'

Proper operation requires the data to be stable for some amount of time before the clock rises → SETUP TIME

Input does not make it through the pass gate

Flip-Flop Timing

- ## D Flip-Flop – T_{SU}
  - ### Setup
  - ### Consider changing D just before the rising edge of clock
    - At a minimum requires the new value to get to N1 before the first pass-gate closes
    - May require as long as it takes for N1' to transition
    - → minimum SETUP time (data stable before rising clock edge)
    - Established by detailed analysis or characterization

stabilizes somewhere in this window
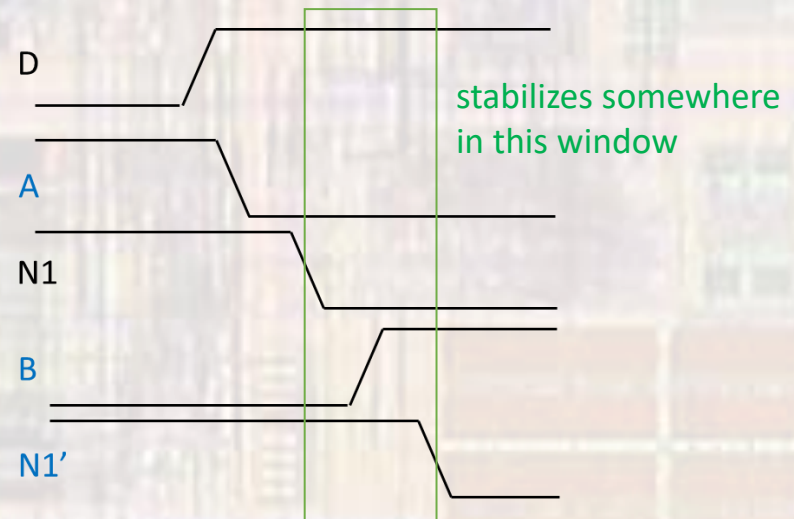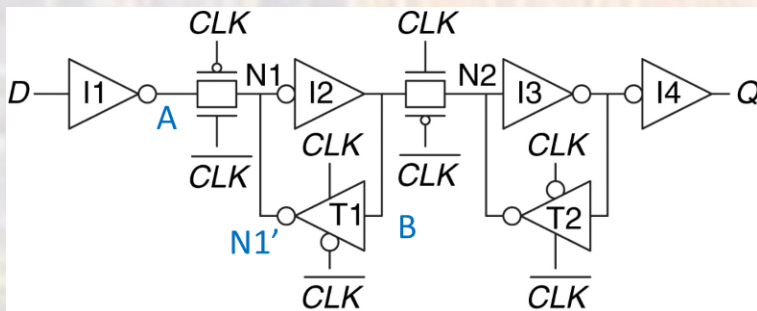
Flip-Flop Timing

- ## D Flip-Flop – T_{HOLD}
  - ### Data changes after Clk ↑

CLK

Pass Gate   Open   Closed

D

case 1

N1

New data gets through even though it changed after the clock

D

case 2

N1

New data is blocked
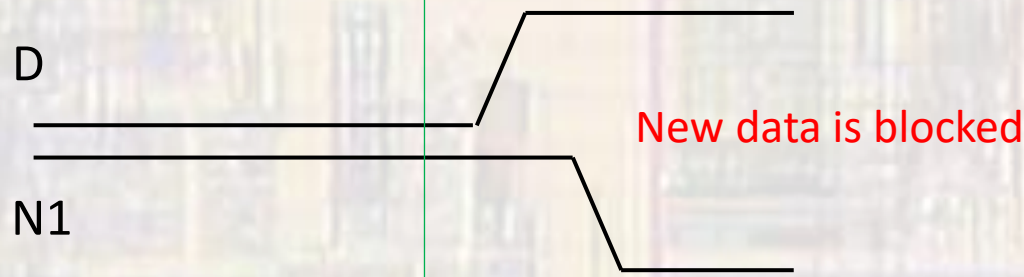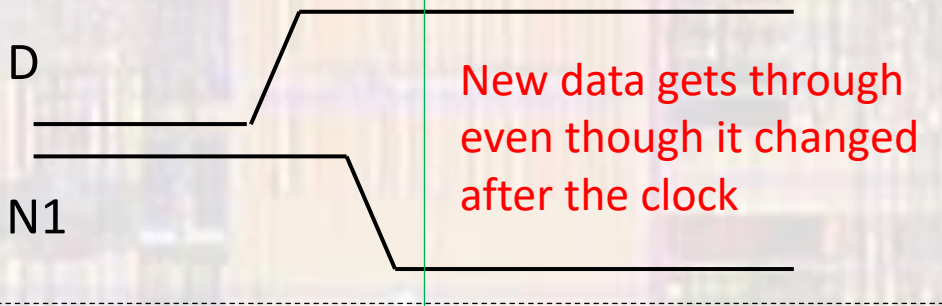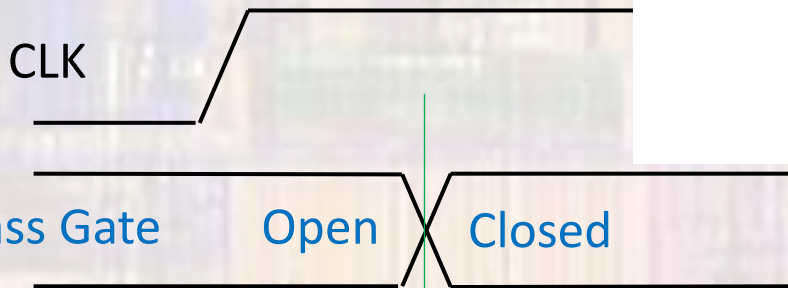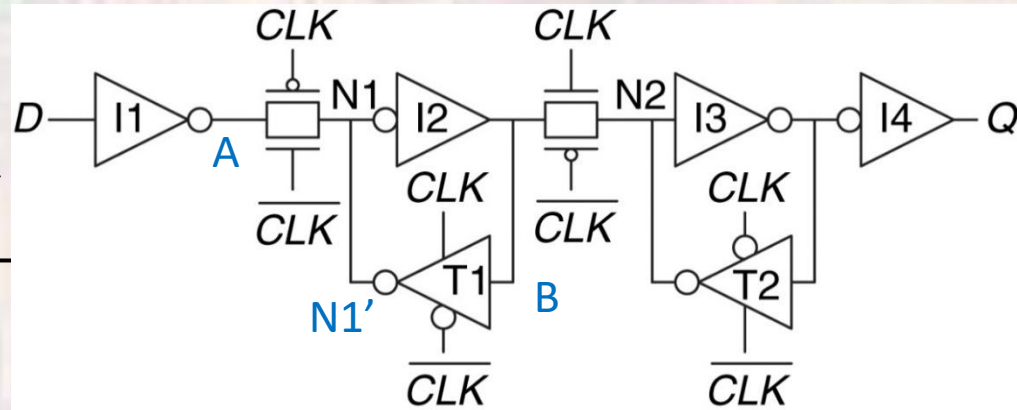
Proper operation requires the data to stay stable for some amount of time after the clock rises → HOLD TIME

Flip-Flop Timing

- ## D Flip-Flop – T_{HOLD}
  - ### Hold
  - ### Consider changing D just after the rising edge of clock
    - Data must stay constant until the pass gate closes
    - $\rightarrow$ minimum HOLD time (data stable after rising clock edge)
    - Note – front end inverter delay complicates this analysis
      - $T_{inv} > T_{pass\ gate} \rightarrow T_{hold} < 0$
    - Established by detailed analysis or characterization
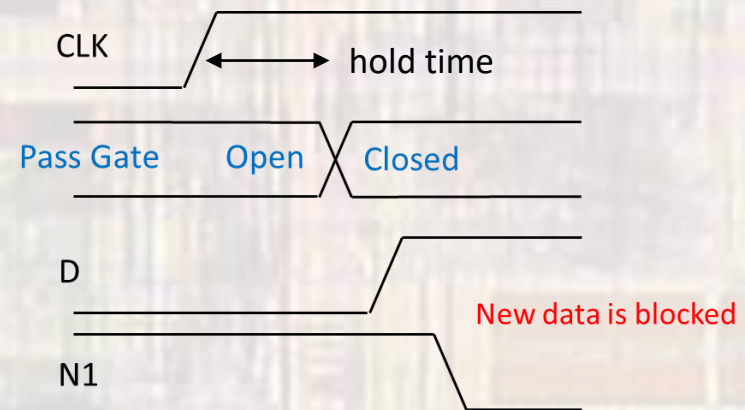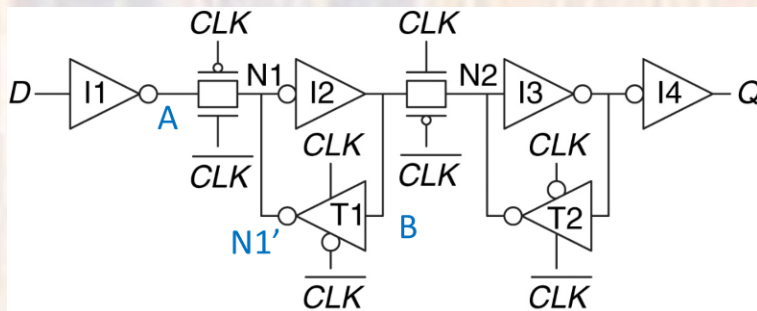
Flip-Flop Timing

- D Flip-Flop

Any D changes in these times
can cause un-predictable results
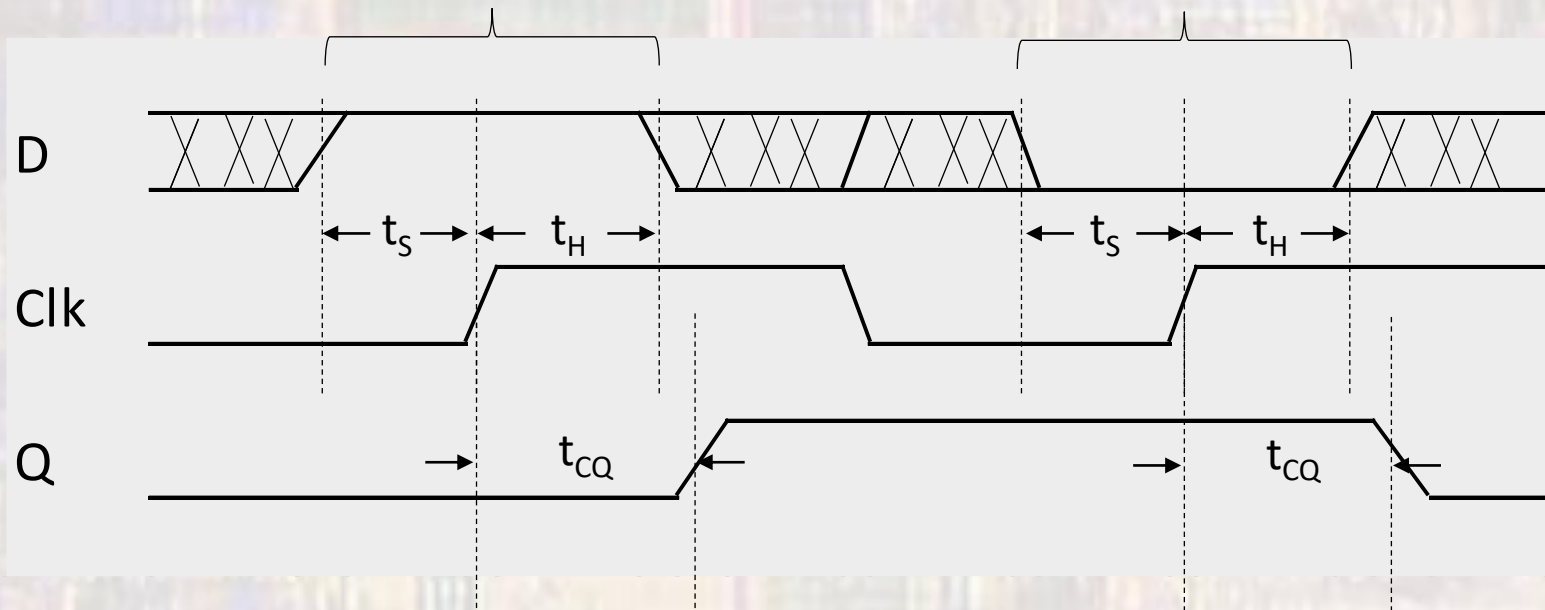
Flip-Flop Timing

- Flip-Flop Timing

    - Other topologies may require different analysis for setup and hold requirements

    - Most designs have a positive setup time and a 0 or negative hold time
        - This allows synchronous system design

Flip-Flop Timing

- CD4013B – CMOS D-FF

6.6 Electrical Characteristics: Dynamic

at T_A = 25°C, input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 20 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}, t_{PLH}	Propagation delay time, clock to Q or $\overline{Q}$ outputs	V_{DD} = 5		150	300	ns
		V_{DD} = 10		65	130	
		V_{DD} = 15		45	90	
t_{PLH}	Set to Q or reset to $\overline{Q}$	V_{DD} = 5		150	300	ns
		V_{DD} = 10		65	130	
		V_{DD} = 15		45	90	
t_{PHL}	Set to $\overline{Q}$ or reset to Q	V_{DD} = 5		200	400	ns
		V_{DD} = 10		85	170	
		V_{DD} = 15		60	120	
t_{THL}, t_{TLH}	Transition time	V_{DD} = 5		100	200	ns
		V_{DD} = 10		50	100	
		V_{DD} = 15		40	80	
f_{CL}	Maximum clock input frequency[1]	V_{DD} = 5	3.5	7		MHz
		V_{DD} = 10	8	16		
		V_{DD} = 15	12	24		
t_W	Minimum clock pulse width	V_{DD} = 5		70	140	ns
		V_{DD} = 10		30	60	
		V_{DD} = 15		20	40	
	Minimum set or reset pulse width	V_{DD} = 5		90	180	ns
		V_{DD} = 10		40	80	
		V_{DD} = 15		25	50	
t_S	Minimum data setup time	V_{DD} = 5		20	40	ns
		V_{DD} = 10		10	20	
		V_{DD} = 15		7	15	
t_H	Minimum data hold time	V_{DD} = 5, 10, 15		2	5	ns

Flip-Flop Timing

- D Flip-Flop

master   slave