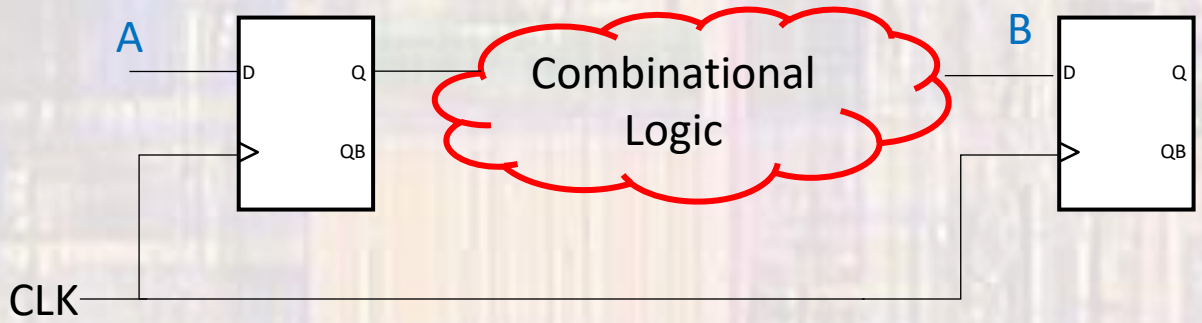
Flip-Flop Timing Analysis

Last updated 2/14/21

Flip-Flop Timing Analysis

- Typical Flip-Flop Circuit

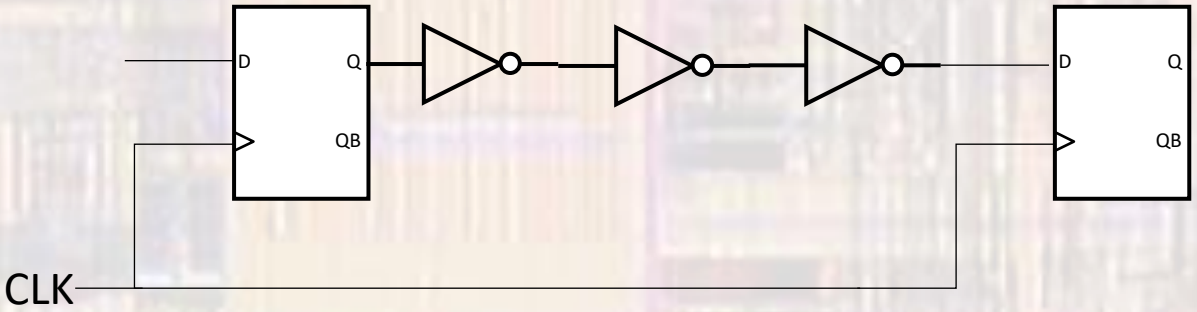


- Need the data to get from point A to point B before the next clock edge occurs

Flip-Flop Timing Analysis

- Flip-Flop Example
  - t_{PD} INV = 10ps
  - t_{CQ} = 22ps
  - t_{setup} = 4ps
  - t_{hold} = 2ps

All values already account for loading

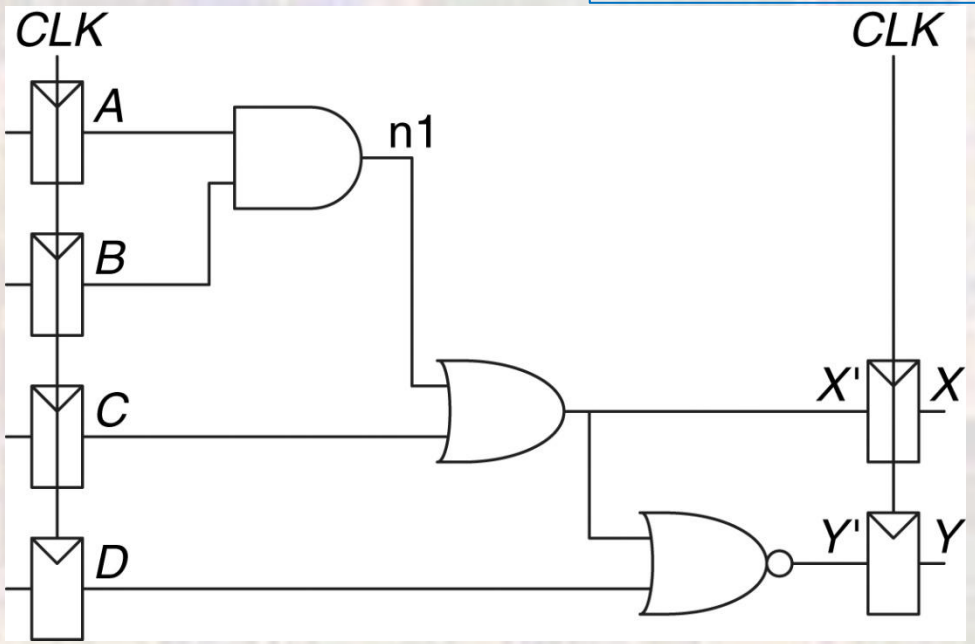


Shortest clock period
Fastest clock speed

Flip-Flop Timing Analysis

- Register Transfer Architecture
  - Timing

All values already account for loading



src: Harris & Harris

t_{CQ_min} = 30ps
t_{CQ_max} = 80ps
t_{setup} = 50ps
t_{hold} = 60ps

t_{pd_min}Logic = 25ps
t_{pd_max}Logic = 40ps

Flip-Flop Timing Analysis

- Register Transfer Architecture
  - Timing

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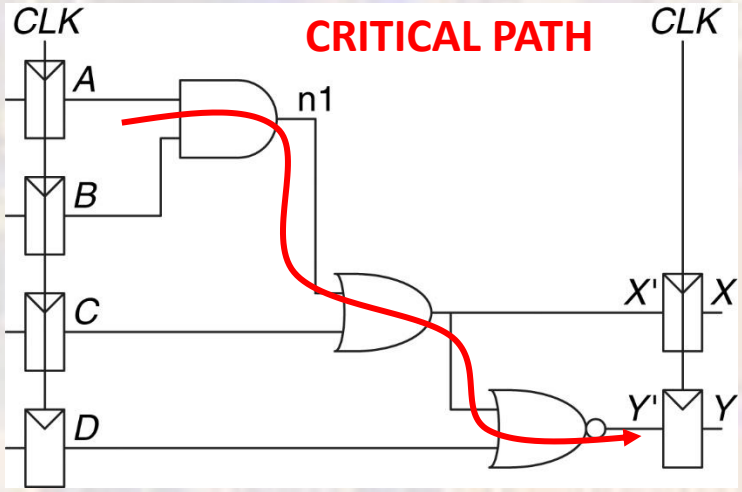

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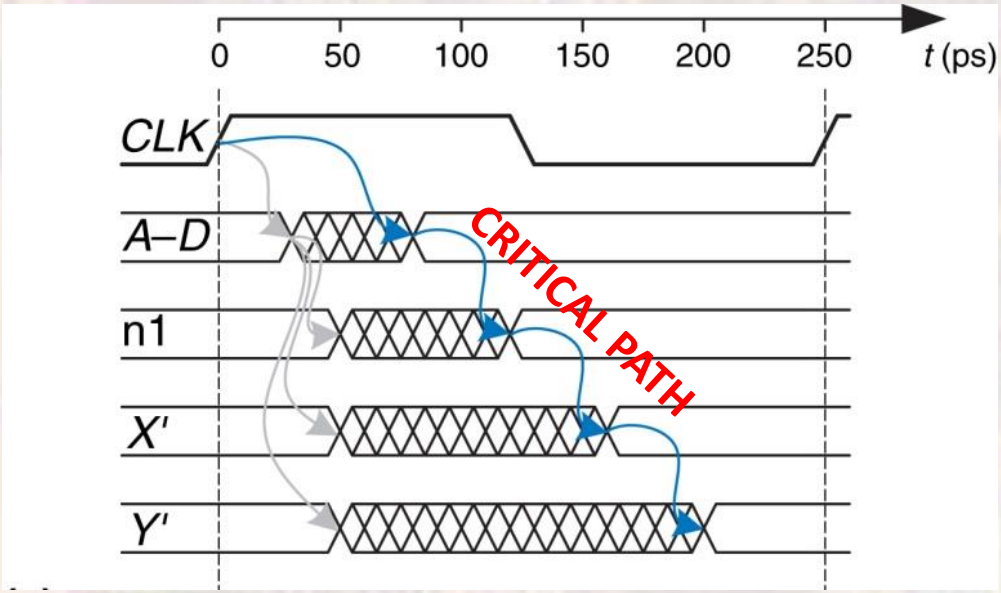

t_{CQ_min} = 30ps
t_{CQ_max} = 80ps
t_{setup} = 50ps
t_{hold} = 60ps

t_{pd_min}Logic = 25ps
t_{pd_max}Logic = 40ps

$$t_{crit} = t_{CQ\_max} + 3*t_{pd\_max} + t_{setup}$$

$$t_{crit} = 80ps + 3*40ps + 50ps = 250ps$$

$$F_{max} = 1/250ps = 4GHz$$

Flip-Flop Timing Analysis

- Register Transfer Architecture
  - Timing

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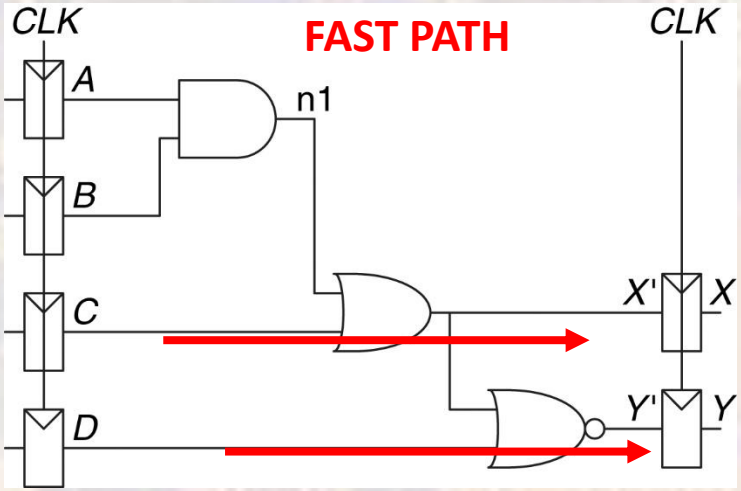

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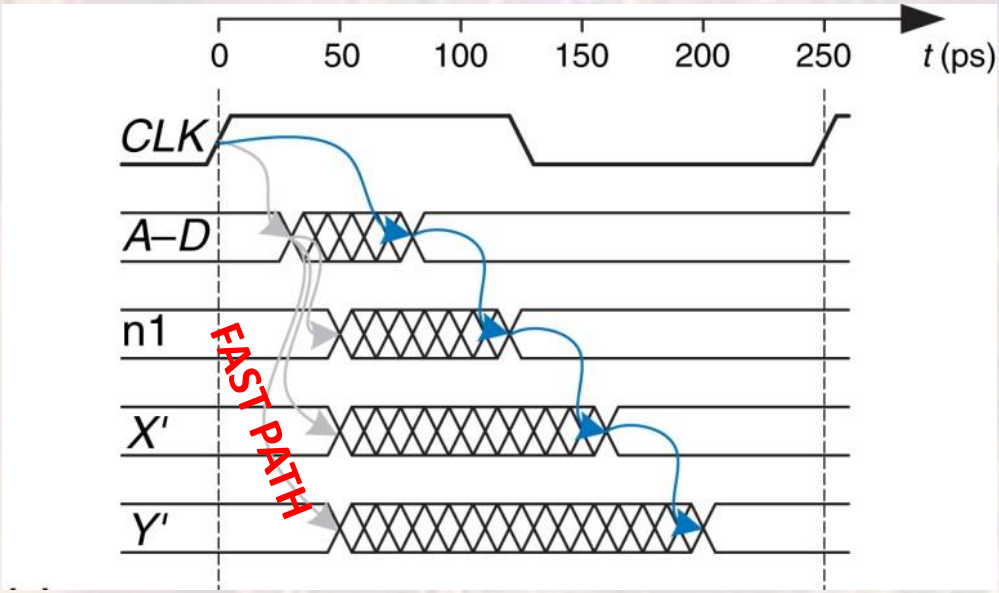

t_{CQ_min} = 30ps
t_{CQ_max} = 80ps
t_{setup} = 50ps
t_{hold} = 60ps

t_{pd_min}Logic = 25ps
t_{pd_max}Logic = 40ps

$t'_{fast} = t_{CQ\_min} + t_{pd\_min}$

t'_{fast} = 30ps + 25ps = 55ps

t'_{fast} < hold time → unpredictable output

Flip-Flop Timing Analysis

- Register Transfer Architecture
  - Timing

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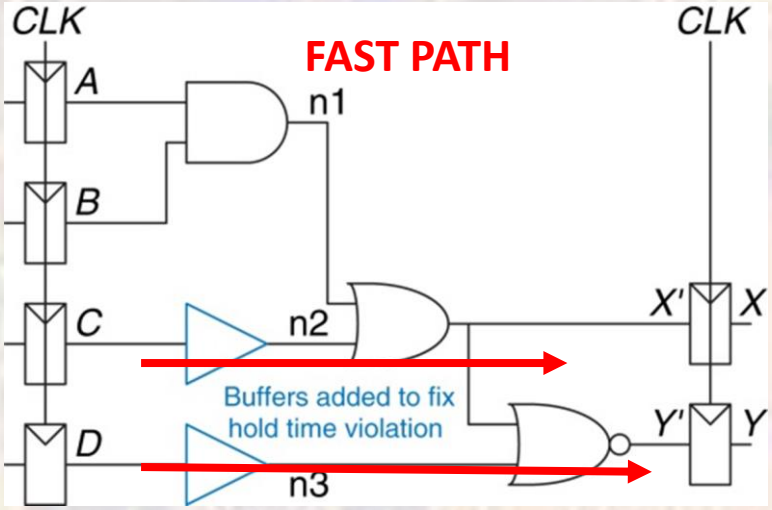

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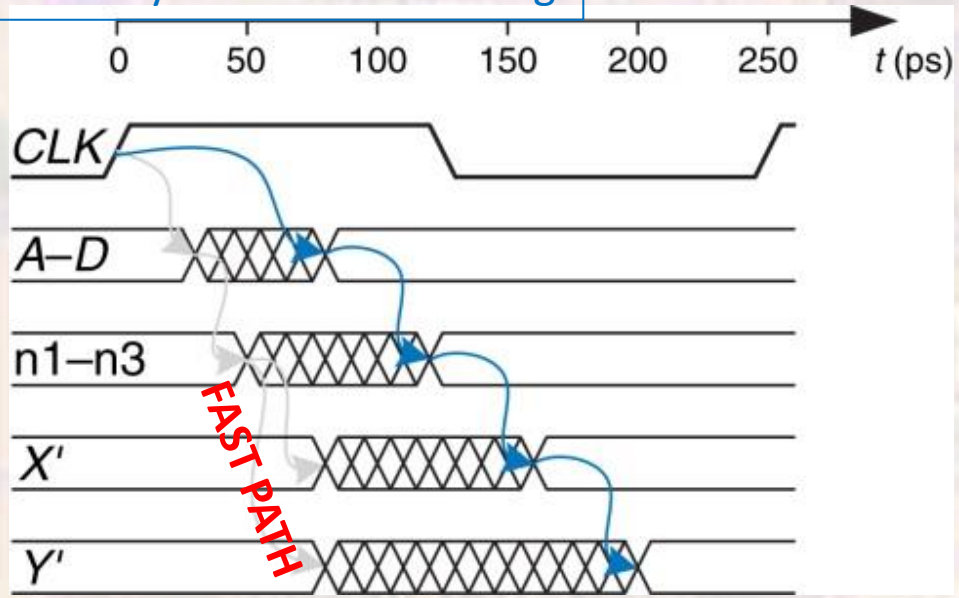


t_{CQ_min} = 30ps
t_{CQ_max} = 80ps
t_{setup} = 50ps
t_{hold} = 60ps

t_{pd_min}Logic = 25ps
t_{pd_max}Logic = 40ps

$t'_{fast} = t_{CQ\_min} + 2*t_{pd\_min}$

$t'_{fast} = 30ps + 2*25ps = 80ps$

t'_{fast} > hold time → predictable output

Flip-Flop Timing Analysis

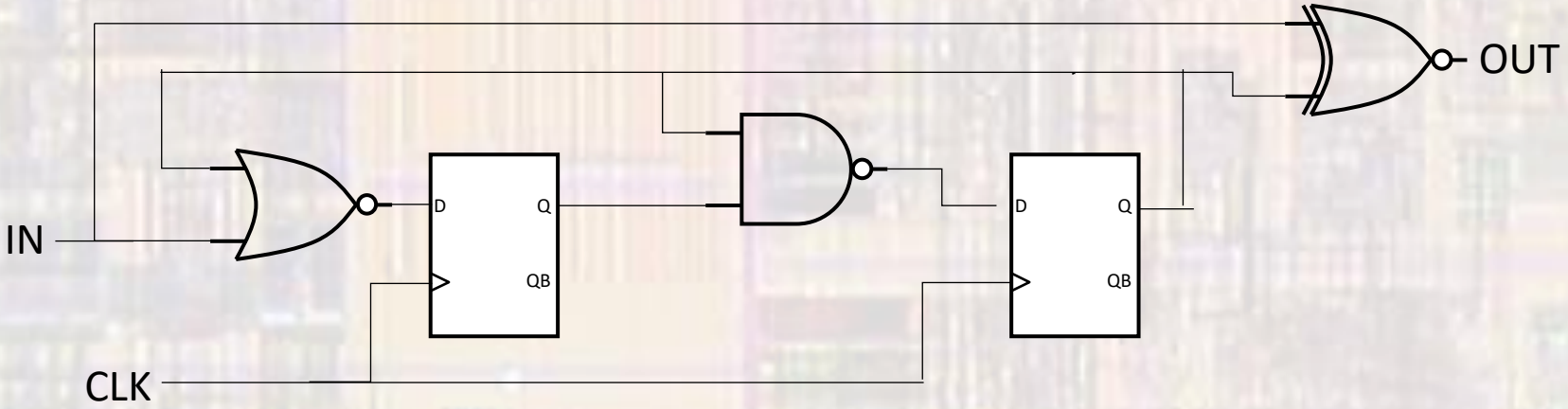
- Additional Timing Issues
  - Clock skew
    - Variation in clock edge arrival time
    - Due to path variations (capacitances)
    - Reduces maximum clock frequency
    - Can create hold time issues
  - Clock Gating
    - Creates clock skew

Flip-Flop Timing Analysis

- Timing Verification
  - Static Timing Analysis
    - Testing for setup and hold violations
    - Check all paths
    - Estimate delays based on worst case assumptions
    - No specific input values are used
    - Logical operation IS NOT checked

Flip-Flop Timing Analysis

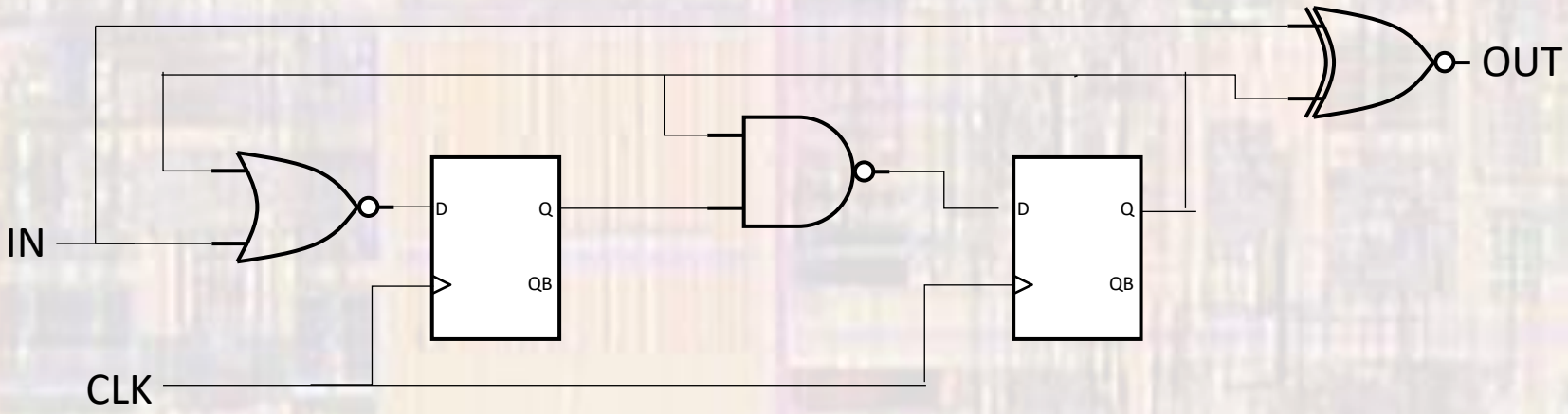
- Timing Verification
  - Static Timing Analysis Path
    - Input of source FlipFlop to Input of destination FlipFlop
    - Input and Output paths



How many static timing paths ?

Flip-Flop Timing Analysis

- Timing Verification
  - Static Timing Analysis Path
    - Input of source FlipFlop to Input of destination FlipFlop
    - Input and Output paths



IN to D1
D1 to D2
D2 to D2
D2 to D1
D2 to OUT
IN to OUT

Flip-Flop Timing Analysis

- Timing Verification
  - Static Timing Analysis Path
    - Input of source FlipFlop to Input of destination FlipFlop
    - Setup time violations
    - Hold time violations
    - Slack – gap between estimated time and violation