HDL Memory Intro

Last updated 1/26/21

HDL Memory Intro

- How can we represent a memory
  - Consider an 8 bit memory structure (1 byte)

  - The 8 bits can be represented by a std_logic_vector

    signal mybyte: std_logic_vector(7 downto 0);

  - Want an array of these
    - Although physically the memory may have multiple columns
    - Logically we will treat the array as one long column

HDL Memory Intro

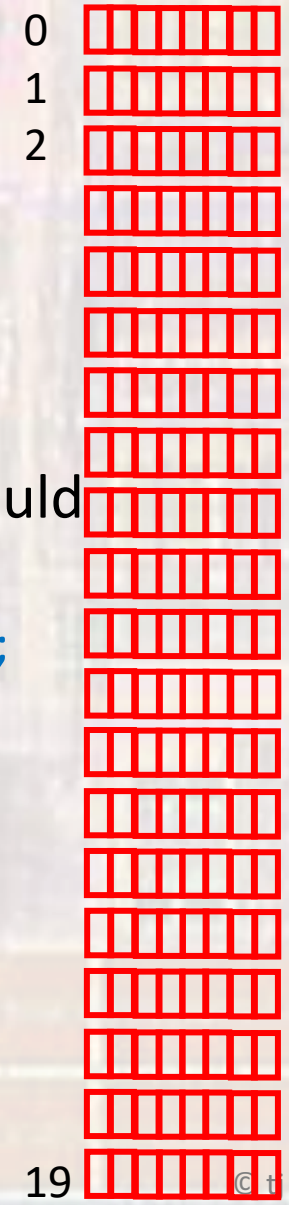
- How can we represent a memory
  - VHDL supports the concept of an array

    type type_name **is array** (range) **of** element_type;
  - A 20 element array of 1 bit values called my_type would be

    type my_type is array (0 to 19) of std_logic;
    - Notice the order of the array
      - We think of the first element of the array as element 0

HDL Memory Intro

- How can we represent a memory



  - VHDL supports the concept of an array

    type type_name **is array** (range) **of** element_type;

  - A 20 element array of 8 bit values called my_type would be

    type my_type is array (0 to 19) of std_logic_vector(7 downto 0);

    - Notice the order of the array
      - We think of the first element of the array as element 0

  - This looks like a memory !