HDL Memory – SRAM MW

Last updated 1/26/21

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- SRAM HDL
  - Quartus has a series of pre-defined blocks
  - They can be created in Quartus - MegaWizard
  - They need to be instantiated in our design

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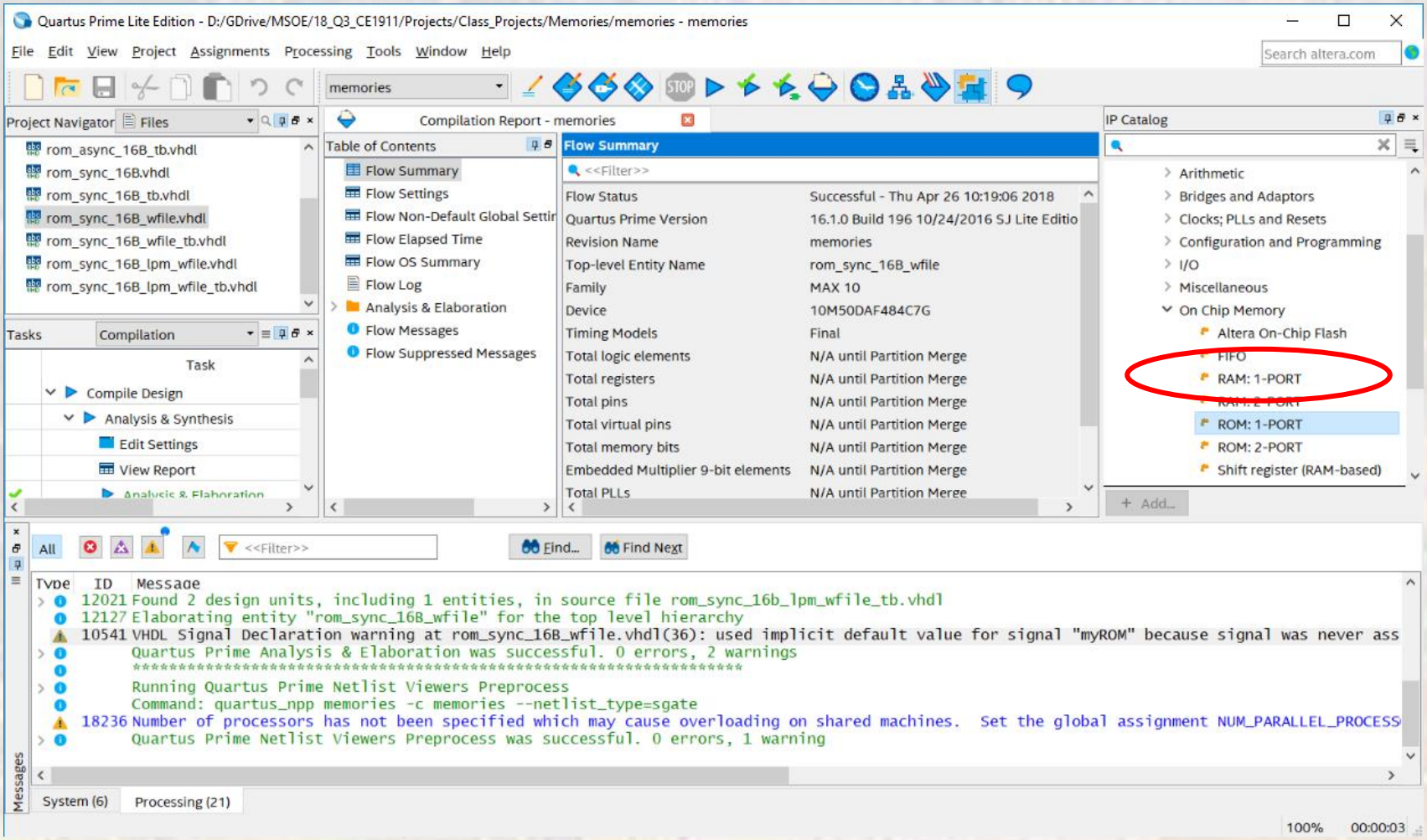
- SRAM HDL - MegaWizard



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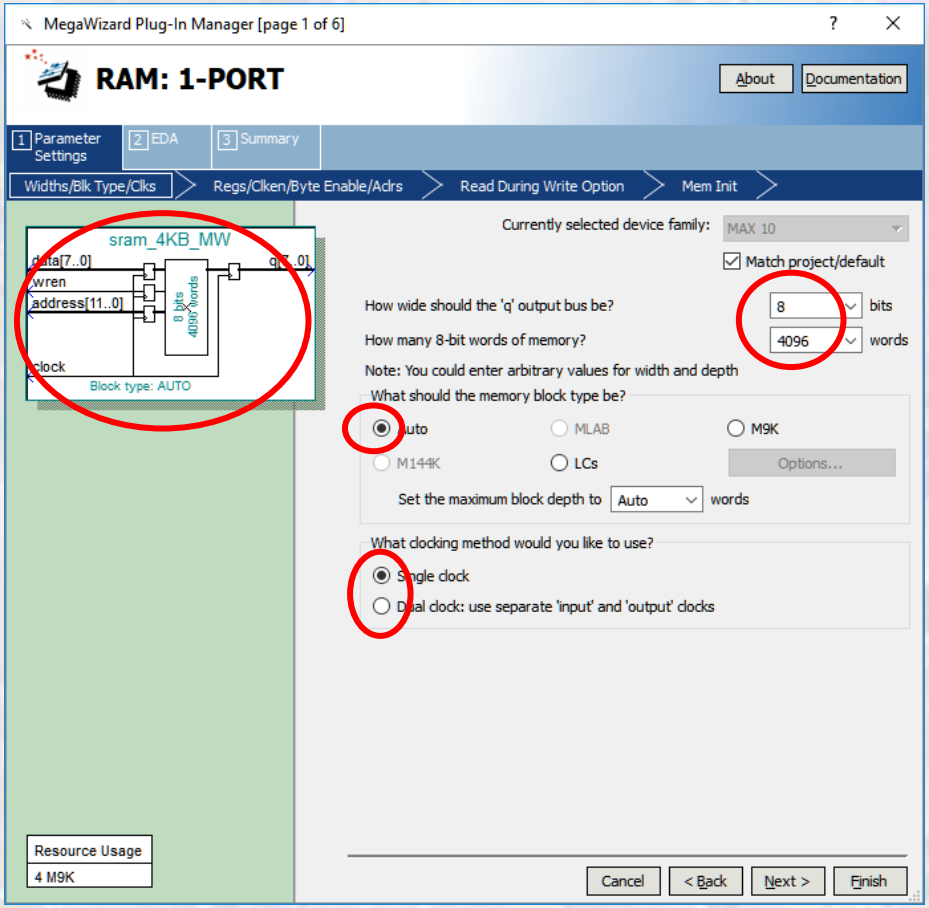
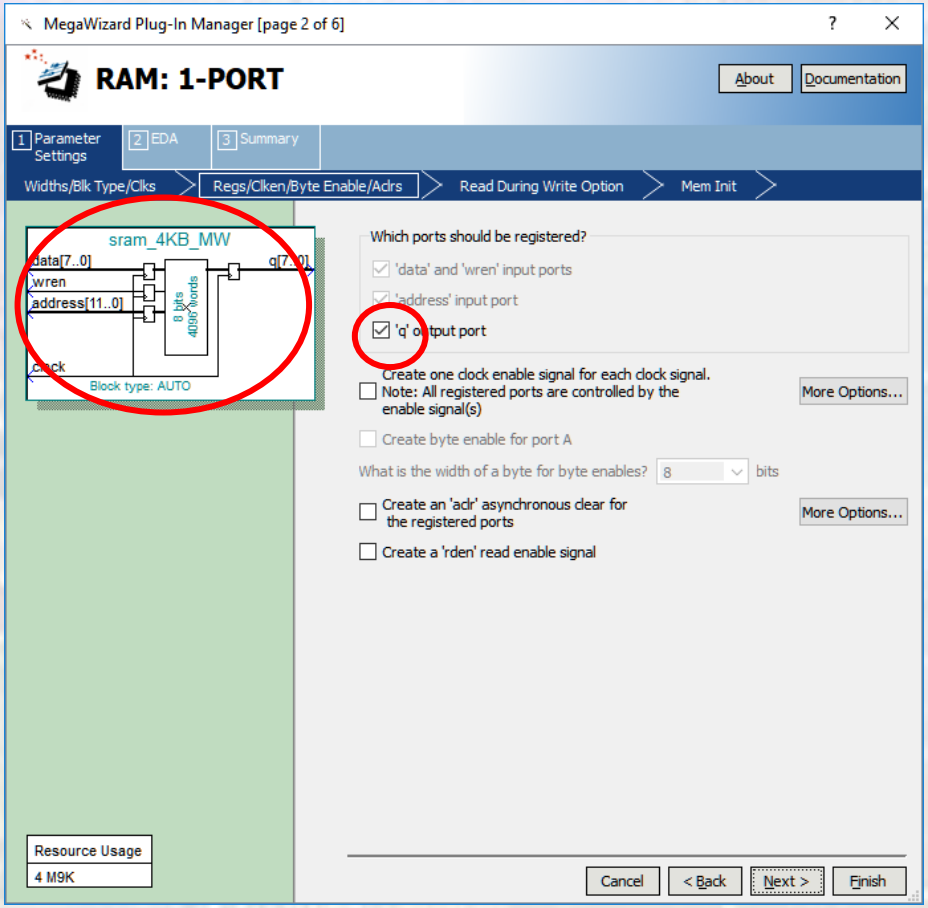
- SRAM HDL – MegaWizard





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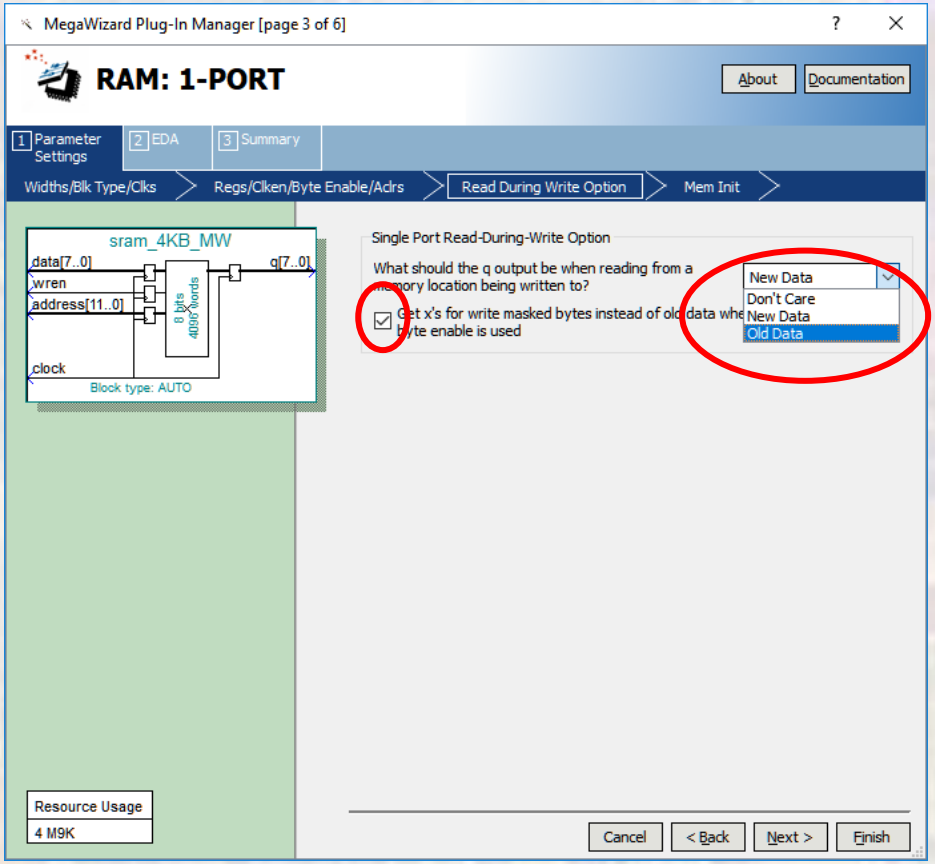

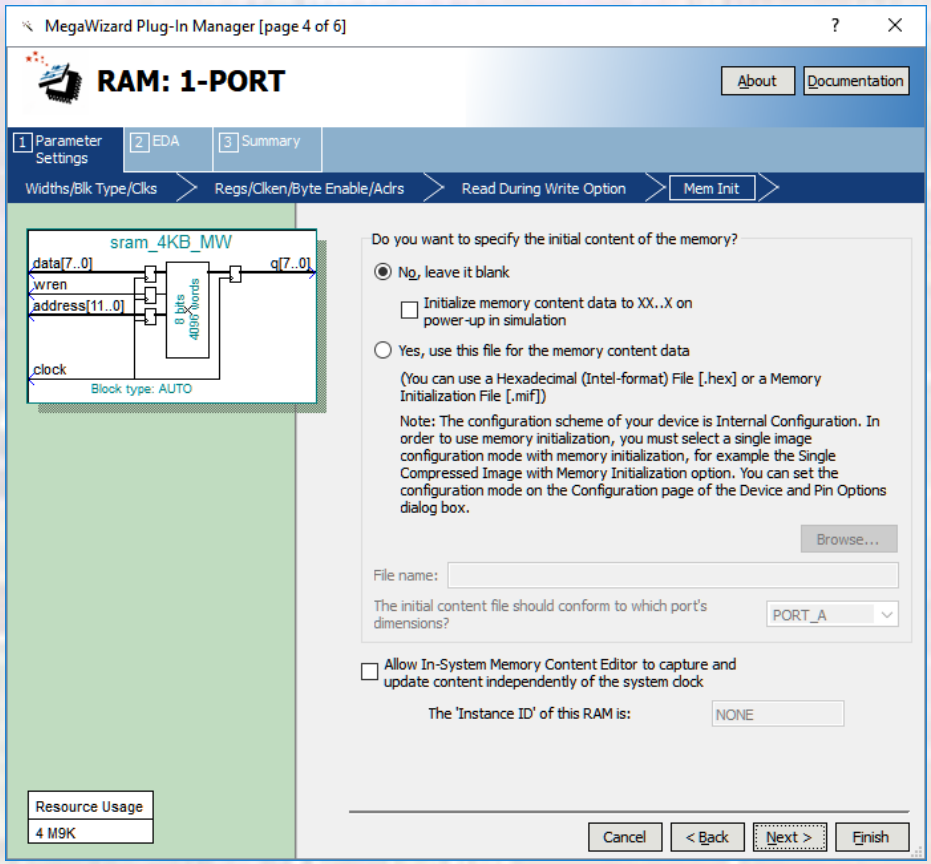

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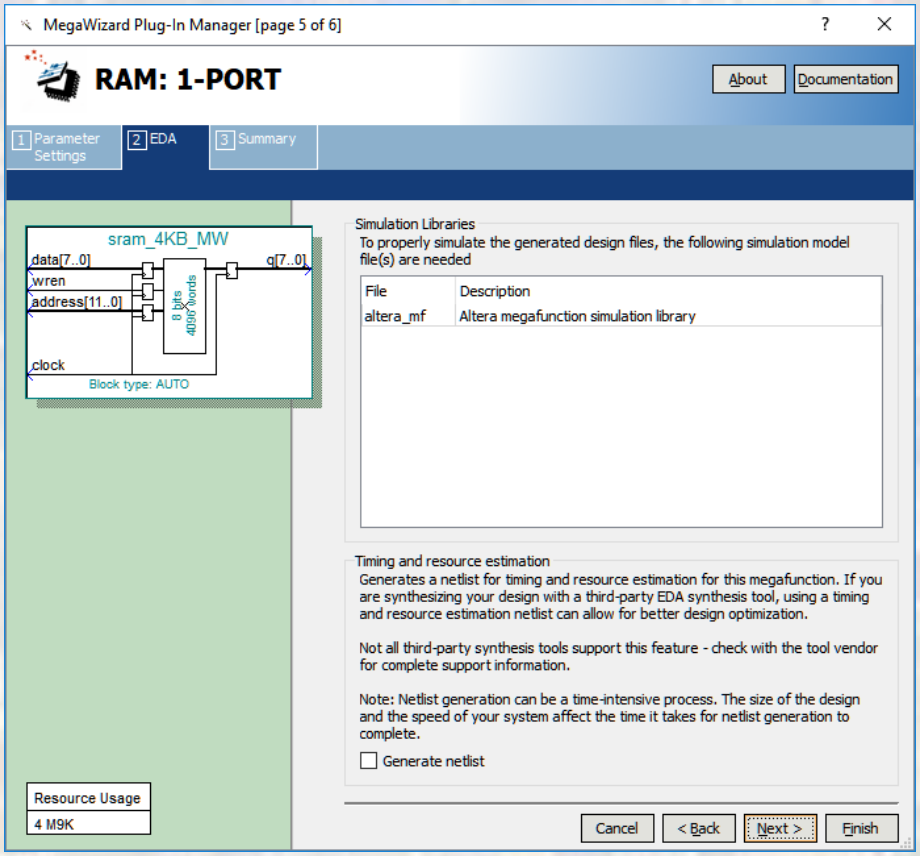

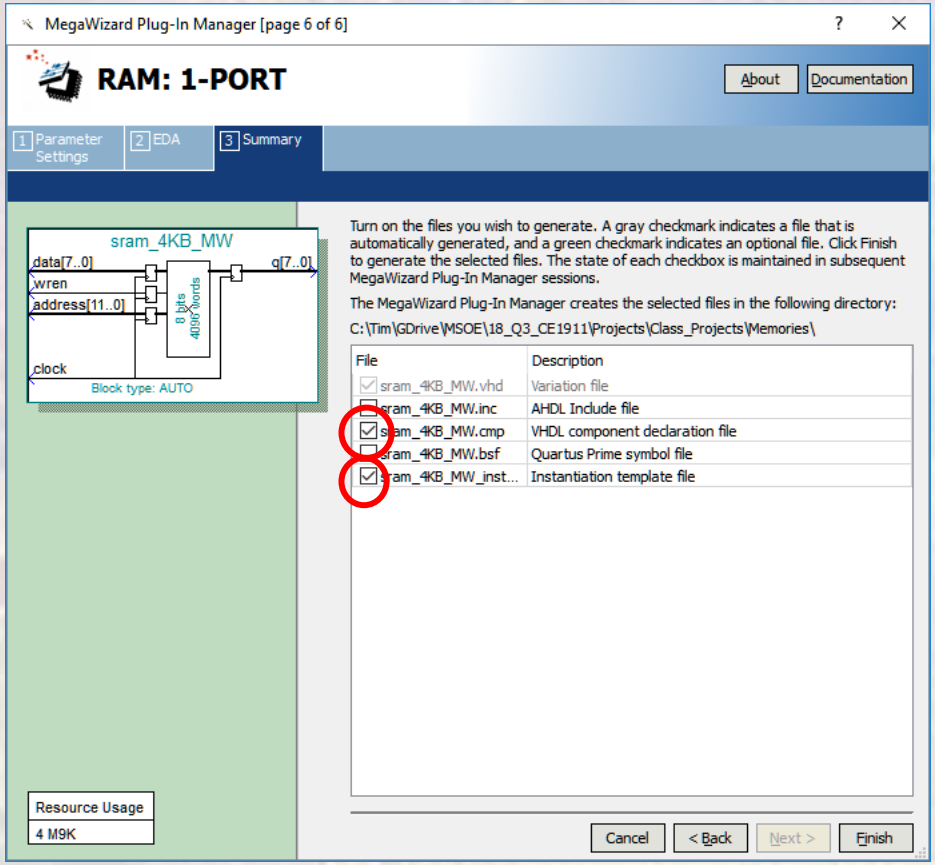

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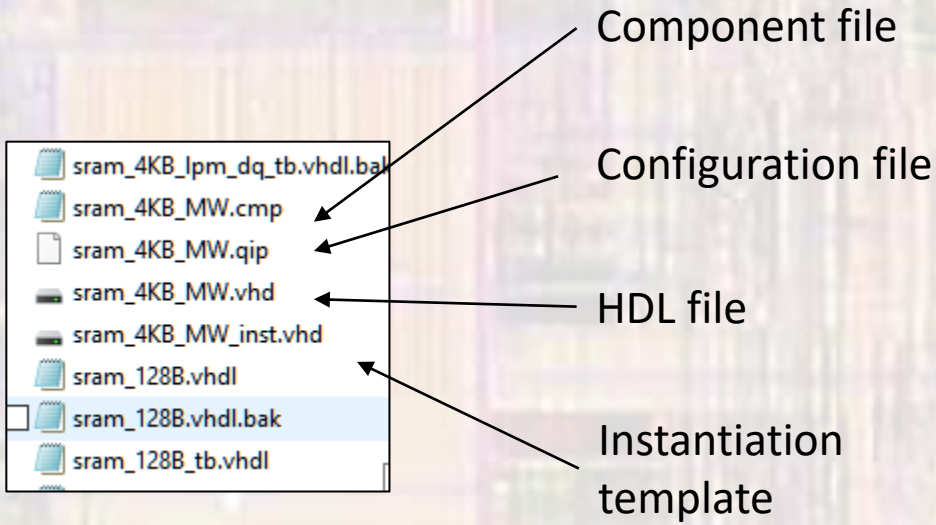
- SRAM HDL - MegaWizard



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System generated HDL file

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;

LIBRARY altera_mf;
USE altera_mf.altera_mf_components.all;

ENTITY sram_4KB_MW IS
    PORT
    (
        address        : IN STD_LOGIC_VECTOR (11 DOWNTO 0);
        clock       : IN STD_LOGIC  := '1';
        data        : IN STD_LOGIC_VECTOR (7 DOWNTO 0);
        wren        : IN STD_LOGIC ;
        q        : OUT STD_LOGIC_VECTOR (7 DOWNTO 0)
    );
END sram_4KB_MW;


ARCHITECTURE SYN OF sram_4kb_mw IS

    SIGNAL sub_wire0  : STD_LOGIC_VECTOR (7 DOWNTO 0);
```

```
BEGIN
    q    <= sub_wire0(7 DOWNTO 0);

    altsyncram_component : altsyncram
    GENERIC MAP (
        clock_enable_input_a => "BYPASS",
        clock_enable_output_a => "BYPASS",
        intended_device_family => "MAX 10",
        lpm_hint => "ENABLE_RUNTIME_MOD=NO",
        lpm_type => "altsyncram",
        numwords_a => 4096,
        operation_mode => "SINGLE_PORT",
        outdata_aclr_a => "NONE",
        outdata_reg_a => "CLOCK0",
        power_up_uninitialized => "FALSE",
        read_during_write_mode_port_a =>
"NEW_DATA_NO_NBE_READ",
        widthad_a => 12,
        width_a => 8,
        width_byteena_a => 1
    )
    PORT MAP (
        address_a => address,
        clock0 => clock,
        data_a => data,
        wren_a => wren,
        q_a => sub_wire0
    );

END SYN;
```

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Component file

```
component sram_4KB_MW
    PORT
    (
        address    : IN STD_LOGIC_VECTOR (11 DOWNTO 0);
        clock      : IN STD_LOGIC  := '1';
        data       : IN STD_LOGIC_VECTOR (7 DOWNTO 0);
        wren       : IN STD_LOGIC ;
        q          : OUT STD_LOGIC_VECTOR (7 DOWNTO 0)
    );
end component;
```

Instantiation template

```
sram_4KB_MW_inst : sram_4KB_MW PORT MAP (
        address    => address_sig,
        clock    => clock_sig,
        data    => data_sig,
        wren    => wren_sig,
        q    => q_sig
    );
```

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```
---------------------------------------
--
-- sram_4KB_MW_ex.vhdl
--
-- created 4/25/17
-- tj
--
-- rev 0
---------------------------------------
--
-- 4KB SRAM from MegaWizard
--
---------------------------------------
--
-- Inputs:  clk, addr
-- Outputs: data
--
---------------------------------------
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity sram_4KB_MW_ex is
   port(
      i_addr       : IN STD_LOGIC_VECTOR (11 DOWNTO 0);
      i_clk        : IN STD_LOGIC;
      i_data_in    : IN STD_LOGIC_VECTOR (7 DOWNTO 0);
      i_we_b       : IN STD_LOGIC;
      o_data_out   : OUT STD_LOGIC_VECTOR (7 DOWNTO 0)

   );
end;
```

```
architecture behavioral of sram_4KB_MW_ex is
   --
   -- we signal
   --
   signal we: std_logic;

component sram_4KB_MW
   PORT
   (
      address   : IN STD_LOGIC_VECTOR (11 DOWNTO 0);
      clock     : IN STD_LOGIC  := '1';
      data      : IN STD_LOGIC_VECTOR (7 DOWNTO 0);
      wren      : IN STD_LOGIC ;
      q         : OUT STD_LOGIC_VECTOR (7 DOWNTO 0)
   );
end component;


begin
   -- we_b mapping
   we <= not i_we_b;

   sram_4KB_MW_inst : sram_4KB_MW PORT MAP (
      address      => i_addr,
      clock        => i_clk,
      data         => i_data_in,
      wren         => we,
      q            => o_data_out
   );

   --
   -- Output logic
   --

end behavioral;
```

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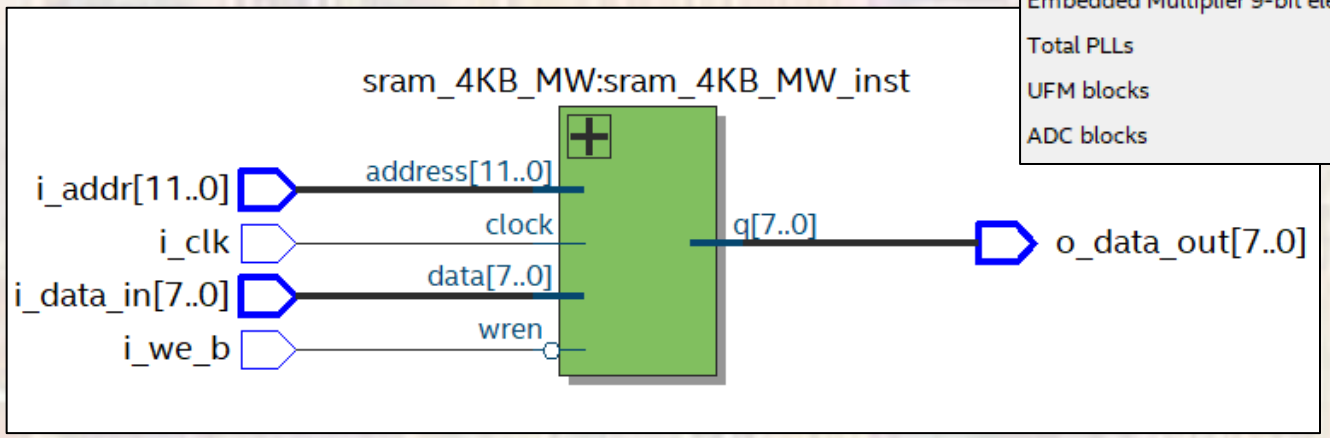
Flow Status	Successful - Tue Jan 28 13:19:53
Quartus Prime Version	18.0.0 Build 614 04/24/2018 SJ L
Revision Name	memories
Top-level Entity Name	sram_4KB_MW_ex
Family	MAX 10
Device	10M50DAF484C7G
Timing Models	Final
Total logic elements	0
Total registers	0
Total pins	30
Total virtual pins	0
Total memory bits	32,768
Embedded Multiplier 9-bit elements	0
Total PLLs	0
UFM blocks	0
ADC blocks	0



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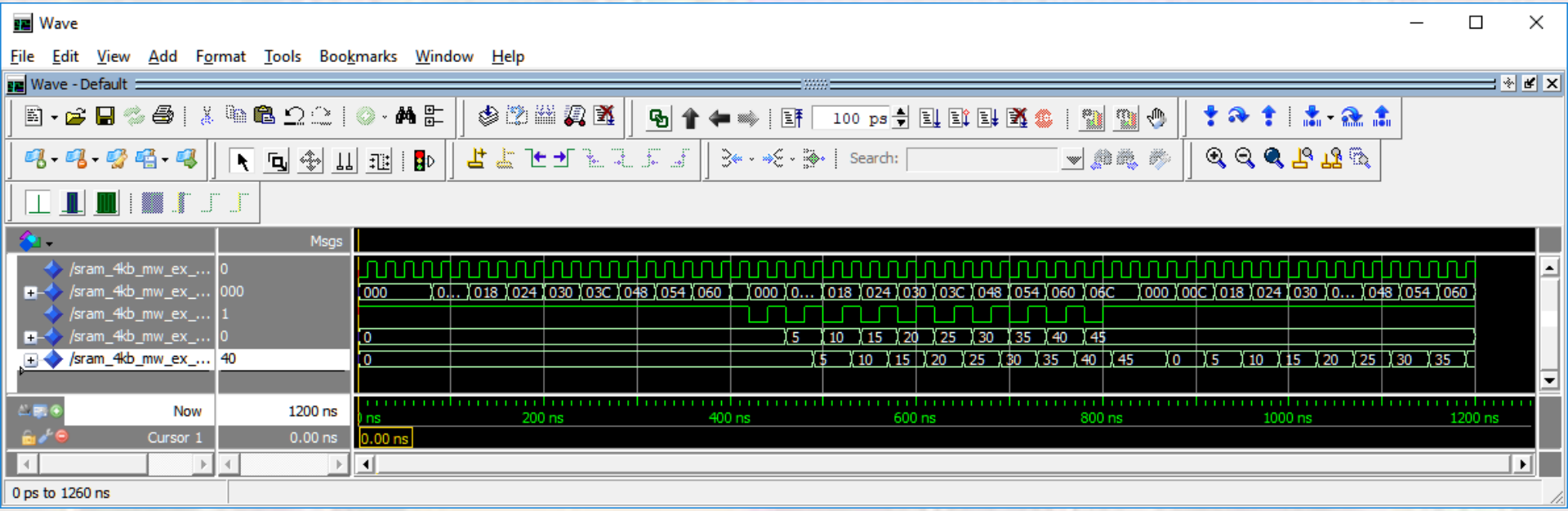
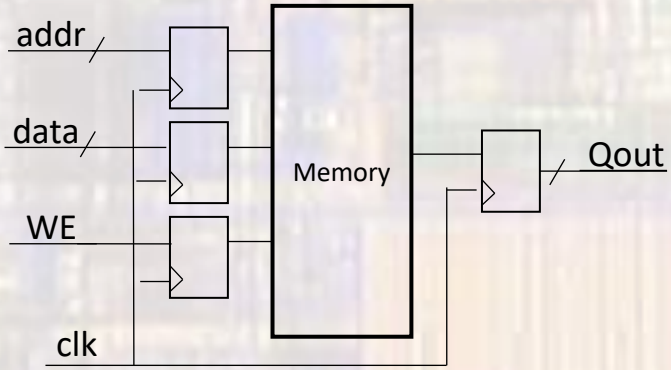
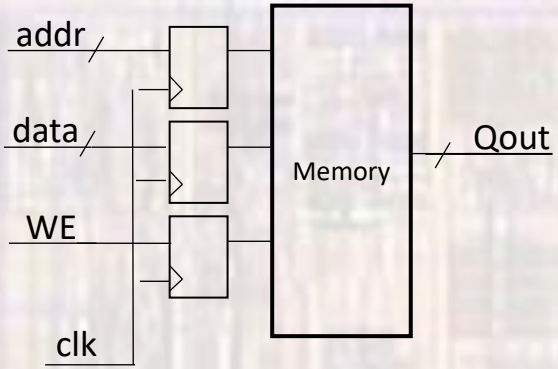
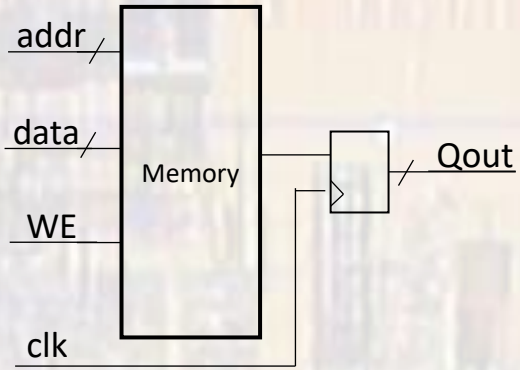


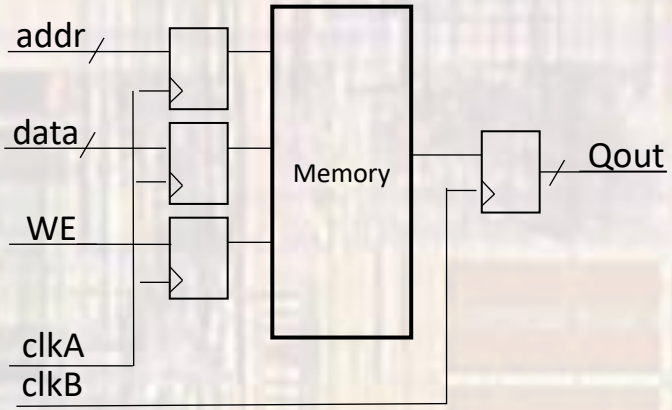
HDL Memory – SRAM MW

- Clock and Register Variations









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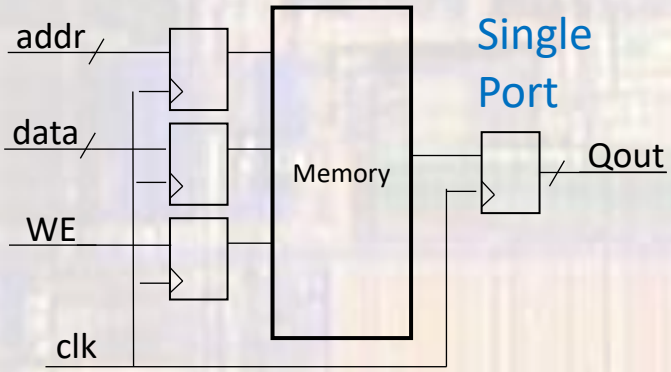
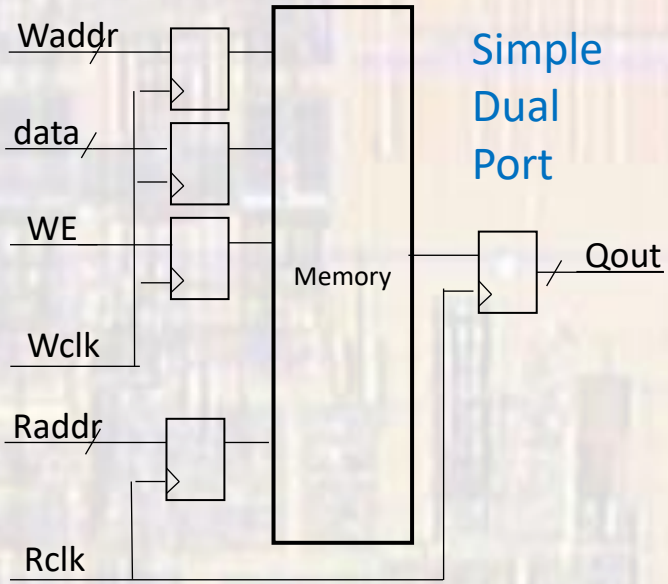
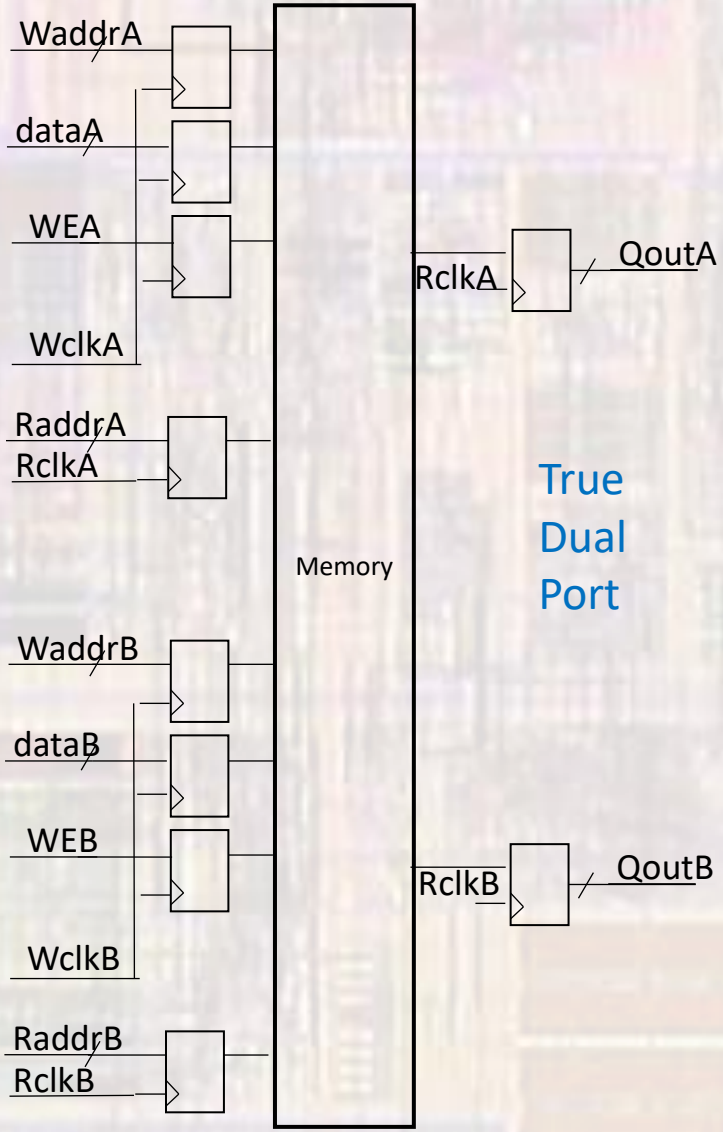
- Port Variations



Single Port



Simple Dual Port



True Dual Port

