CE 1911

Homework 3

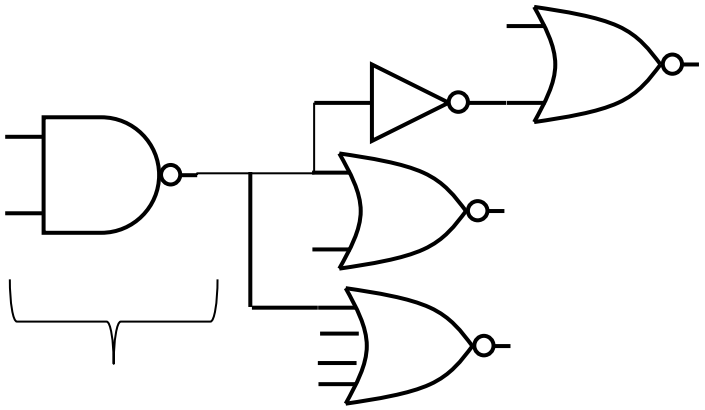
1 – Given the gate information below, calculate the t_{pd} for the 2 input nand gate

** we are assuming interconnect capacitance is negligible

30pts

Gate	INV	2-NAND	2-NOR	4-NAND	4-NOR
Input load factor	0.8	1.0	1.0	1.75	1.75
Fixed delay factor	50ps	65ps	65ps	80ps	80ps
Variable delay factor	5ps	8ps	8ps	12ps	12ps

$t_{pd} = t_{fixed} + t_{variable\_factor} *$ Load Equivalents



2 – Given the gate information below, calculate the t_{pd} for the 2 input nand gate 30pts

** we are assuming interconnect capacitance is negligible

Gate	INV	2-NAND	2-NOR	4-NAND	4-NOR
Input load factor	0.8	1.0	1.0	1.75	1.75
Fixed delay factor	50ps	65ps	65ps	80ps	80ps
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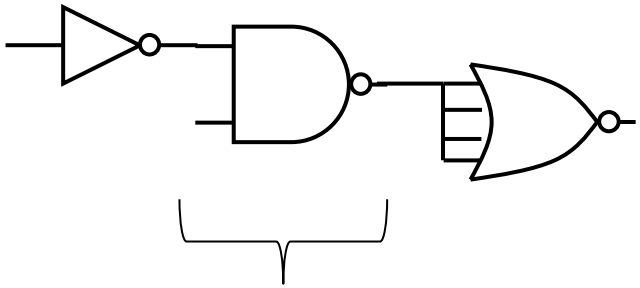
$t_{pd} = t_{fixed} + t_{variable\_factor}$* Load Equivalents



3 – Calculate the fastest possible clock frequency 40pts

t_{PD} INV = 10ps
t_{PD} NAND = 15ps
t_{CQ} = 20ps
t_{setup} = 5ps
t_{hold} = 2ps