Elevator Lab

Objectives:

This lab was focused on creating a FSM design for an elevator controller. One of the major goals was to create a single design that could be used for an elevator with any number of floors, both above and below ground level.

Procedures:

The prelab portion of the lab required me to review both the FSM notes and the VHDL notes on case statements. I first created a paper design using a state diagram map. The final version of the paper design is shown in fig. 1.

I then coded the design in VHDL using a state/next state approach and a case statement. The commented code is shown in fig. 2. Key elements of the design are the inputs: button and current floor number, a timer to set the wait time for the open doors, the outputs: move, and open/close, and the states: idle, up, down, wait, return.

After completing the design I developed a series of test benches (fig. 3-6) and ran a series of 4 simulations to test the operation of the design. The initial design failed to return to the first floor, leading to modifications of the state machine. Once these modifications were made the design simulated successfully. The annotated simulations are shown in figures 7 – 10.

Once the design was verified I created a DE10 top level (fig. 11) where I instantiated my elevator design and a clock divider to slow down the system operation. This was then compiled and loaded onto the DE10 Lite board. I ran the required test scenarios for check off.

Results:

All six test bench simulations ran successfully.

Test bench 1 validated that the up/down functionality is correct (see fig. 7).

Test bench 2 validated the wait at floor functionality (see fig. 8).

Test bench 3 shows that the return to the lobby functionality works (see fig. 9).

Test bench 4 confirmed a complex scenario using a series of inputs (see fig. 10).

When the design was moved to the DE10 a subset of the full test benches was run to confirm operation. The subsets are listed in fig. 12. All completed successfully.

Observations and Conclusions:

This project taught me to focus on generalizing the functionality of a design to reduce the overall complexity of the circuitry. I also found that I can run many more simulations than DE10 examples in a given period of time.

Appendix and References:

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