CE 1911 Week 2 Lab: Synchronous Schematic Design

Name:_____

Objectives

- Design simple synchronous circuits by hand
- Review schematic capture and simulation in Quartus
- Create a test-bench verification solution

Prelab **student check off**

- Create a working directory and project in Quartus for W2Lab ☐
- Create a 4 bit up counter schematic (jk version just like in the notes) ☐
  - Call it: counter_4bit.vhdl
  - Pin names: i_clk, i_rstb, o_b0, o_b1, o_b2, o_b3
- Review the test bench slides ☐

Assignment

Part 1: **Design a 4 bit up counter with asynchronous reset.**

We will do this together

1) Create the schematic (prelab requirement)
2) Convert the design to HDL
3) Create a test bench to verify the counter
4) Run a simulation using your test bench

Part 2: **Design a 4 bit shift L/R shift register**.

1) Create the schematic (like in the notes but 4 bit)
   a. You will want to create a 4-1 mux component to use
   b. Call it: shift_reg_4bit
   c. Pin names: i_clk, i_rstb, i_sel[1..0], i_din, o_b0, o_b1, o_b2, o_b3
2) Convert the design to HDL
3) Create a test bench (or 3 if you prefer) to verify the counter
   a. A testbench is provided – you may need to change the names
   b. Shift a 1 all the way through the shift register
   c. Shift a 1 to the end and then back
   d. Shift a continuous 1 – 0 pattern through the shifter
4) Run simulations using your test bench

Check Off

- Demo and document your up counter schematic and simulation 40%
- Demo and document your shift register schematic and simulations 60%

Lab Report (informal)

- Due at 4:00 pm, Monday after lab – in the box
- Include a properly documented informal lab report.