CE 1911 Week 3 Lab: Synchronous HDL Design

Name:_____

Objectives

- Design simple HDL based structures

Prelab **student check off**

- Review the HDL design notes ☐

Assignment

Part 1: **Design a 3 bit unsigned up/down non-wrapping counter with asynchronous reset**. Non-wrapping means the counter does not wrap-around to 0 after reaching 7 when counting up, and does not wrap-around to 7 after reaching 0 when counting down. In both cases it remains in the terminal state until the direction is changed. UP: 0-1-2-…-6-7-7-7-7 … DOWN: 7-6-… -1-0-0-0-0 … UP: 0-1-2…
Use the provided test bench to verify your design.
Be sure to check the provided testbench for block and signal names

Part 2: **Design a 3 bit unsigned odd/even wrapping counter with asynchronous reset.** This counter should count up with even numbers and down with odd numbers. UP: 0-2-4-6-0-2…, DOWN: 7-5-3-1-7-5… Note when transitioning from UP to DOWN or DOWN to UP the counter will only step 1 number. 0-2-4-6/DOWN/5-3-1/UP/2-4-6.
Create a test bench to verify your design.
Be sure to check the provided results plot for testbench expectations

Part 3: **Design an N bit unsigned odd/even non-wrapping counter with asynchronous reset.**
(Repeat the design of part 2 but with a non-wrapping solution)
Create a test bench to verify your design (use N = 4).
Be sure to check the provided results plot for testbench expectations

Check Off

Be sure to simulate/demonstrate both reset conditions and multiple direction changes

- Demo and document your 3 bit unsigned up/down non-wrapping counter test bench 30%
- Demo and document your 3 bit unsigned odd/even wrapping counter test bench 40%
- Demo and document your N bit unsigned odd/even non-wrapping counter test bench 30%

Lab Report (informal)

- Due at 4:00 pm, Monday after lab – in the box
- Include a properly documented informal lab report.