CE 1911 Week 4 Lab: Advanced HDL Design

Name:_____

Objectives

- Design a complex HDL component
- Implement the design on the DE10

Prelab **student check off**

- Create a working directory and project in Quartus for W4Lab ☐

Assignment

Part 1: **Design an N bit count by M up/dn counter.**

Design an N bit counter that counts up or down by an increment specified by an M bit input signal.

Signals:

clk, rstb

run – 1 bit – input - (0 for hold current value, 1 for count)

dir – 1 bit – input - (0 for up, 1 for down)

incr – M bits – input - vector representing amount to increment(dec) the count

count – N bits – output – current count

E.g. M = 4 would allow increments/decrements of 0 to 15

Create a test bench and verify your design using N = 16, M = 4.

Be sure to check the provided results plot for testbench expectations

Part 2: **Implement your counter on the DE10 with N = 8, M = 3.**

Create a DE10 implementation of your design with a 1Hz clock

Create a vhdl file for your DE10 implementation

Instantiate your design in a DE10 vhdl implementation

Instantiate the 1Hz clock (so we can see the LEDs changing)

Use CLOCK_50 for the clock

Use switches (6) for the inputs (except clk)

Use LEDs (8) for count

Check Off

- Demo and document your 16/4 counter schematic and simulation 50%
- Demo and document your DE10 implementation (instructor will provide inputs) 50%

Lab Report (informal)

- Due at 4:00 pm, Monday after lab – in the box
- Include a properly documented informal lab report.