CE 1911 Week 5 Lab: FSM Schematic Design

Name:_____

Objectives

- Design simple Finite State Machines by hand
- Review schematic capture and simulation in Quartus

Prelab **student check off**

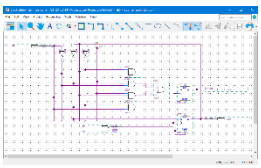
- Create a working directory and project in Quartus for W5Lab ☐
- Review the FSM design slides ☐

Assignment

Part 1: **Design a 2 bit up/down counter with asynchronous reset.**

1) Identify the states
2) Identify the inputs and outputs
3) Assign values for the inputs and outputs (use simple binary encoding)
4) Create a state transition diagram
5) Create a state transition table
6) Create truth tables for the next state and output logic
7) Minimize the next state and output logic
8) Create the schematic in Quartus – no HDL
9) Create a Test bench and verify all state transitions and outputs

   Be sure to check the provided results plot for testbench expectations

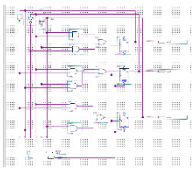


Part 2: **Design a 3 bit Gray Code counter with asynchronous reset.**

Gray code counters count: 0-1-3-2-6-7-5-4-0-1… (only 1 bit changes each count)

Use the same process as in part 1 – no HDL.

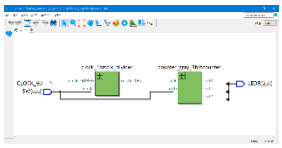
Be sure to check the provided results plot for testbench expectations



Create a DE10 implementation of your design with a 1Hz clock

Instantiate your design in a DE10 vhdl implementation (using 3 leds)

Instantiate the 1Hz clock (so we can see the LEDs flashing)



Check Off

- Demo and document your 2 bit up/down counter schematic and simulation 50%
- Demo and document your 3 bit Gray Code counter schematic, simulation, and DE10 50%

Lab Report (informal)

- Due at 4:00 pm, Monday after lab – in the box
- Include a properly documented informal lab report.