CE 1911 Week 6 Lab: FSM HDL Design

Name:_____

Objectives

- Design a moderately complex Finite State Machines using VHDL
- Develop a DE10 implementation using switches and seven segment displays

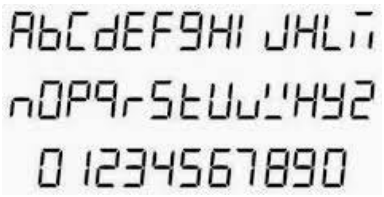
Prelab	**student check off**
• Create a working directory and project in Quartus for W6Lab	☐
• Review HDL FSM class notes	☐
• Review CE1901 notes on using the seven segment displays	☐
• Create a state transition diagram for your design	☐

Assignment

Part 1: **Create and simulate a full function stoplight system using a timer based FSM.**

1) Normal operation cycles from
   RR – 1 clk, RG – 7 clks, RY – 3 clks, RR – 1 clk, GR – 7 clks, YR – 3 clks, …
2) Maintenance mode – solid RR based on signal "maint"
3) Power fail mode – flashing RR (1 clk on, 1 clk off) based on signal "pwr_fail"
4) Emergency vehicle mode – **safely** transition to GR or RG in direction A or B based on 2 signals "emergency_A" or "emergency_B"
5) Use the following priority – power fail >> maintenance >> emergency >> normal

Be sure to check the example simulation plot for testbench expectations



Part 2: **Implement your design on the DE10 board.**

Use a 3Hz clock divider to slow down the clock
Use switches as the control inputs
Use 3 LEDs for each direction A and B
Use 4 seven segment displays to indicate the status of your system using letters
Normal operation – 2 sseg for each direction (A and B) – rd, ye, gr
Maintenance mode – main
Power out mode – fail – flashing
Emergency vehicle mode – em in the emergency direction, normal operation in the second direction

Check Off

- Demo and document your stoplight schematic and simulation 50%
- Demo and document your DE10 implementation 50%

Lab Report (informal)

- Due at 4:00 pm, Monday after lab – in the box
- Include a prope ly documented informal lab report.