CE 1911 Week 8 Lab: Memory HDL Design

Name:_____

Objectives

- Design a memory using VHDL
- Develop a DE10 implementation using switches and seven segment displays

Prelab	**student check off**
• Create a working directory and project in Quartus for W8Lab	☐
• Review HDL Memory class notes	☐
• Review CE1901 notes on using the seven segment displays	☐

Assignment

Part 1: Create a ROM using the MegaWizard single port ROM. The ROM should be 256b in a by 8 configuration. The ROM data should consist of hex values based on transposing the address nibbles. E.g. addr = 0x00 → data = 0x00, addr = 0x2F → data = 0xF2, addr = 0x17 → data = 0x71, …

Implement the address input with switches (and display with 2, 7-segment displays) and the data output with 2, 7-segment displays.

Part 2: Create a Single port RAM using the inferred method (no library elements). The RAM should be 32 x 8b.

Implement the address input with switches (and display with 2, 7-segment displays) and the data output with 2, 7-segment displays. Use 4 switches for the data input. Use a switch for a write_enable_bar signal. Use a key for rstb (for the clock divider)

Check Off

• Part 1: Demo and document your simulation and DE10 implementation	50%
• Part 2: Demo and document your simulation and DE10 implementation	50%

Lab Report (informal)

- Due at 4:00 pm, Monday after lab – in the box
- Include a properly documented informal lab report.