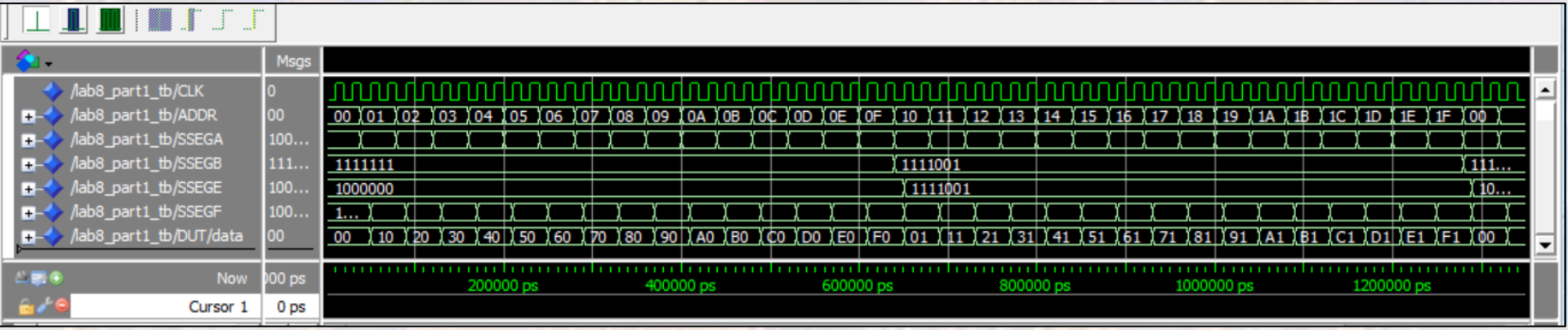
Lab8 – Part1

```
entity lab8_part1 is
   port(
      i_clk:          in    std_logic;
      i_addr:         in    std_logic_vector(4 downto 0);
      o_addr_sseg_A: out    std_logic_vector(6 downto 0);
      o_addr_sseg_B: out    std_logic_vector(6 downto 0);
      o_data_sseg_E: out    std_logic_vector(6 downto 0);
      o_data_sseg_F: out    std_logic_vector(6 downto 0)
   );
end entity;
```




```
entity lab8_part1_de10 is
   port(
         CLOCK_50:    in    std_logic;
         SW:          in    std_logic_vector(5 downto 0);

         HEX0:        out   std_logic_vector(6 downto 0);
         HEX1:        out   std_logic_vector(6 downto 0);
         HEX4:        out   std_logic_vector(6 downto 0);
         HEX5:        out   std_logic_vector(6 downto 0)
   );
end entity;
```