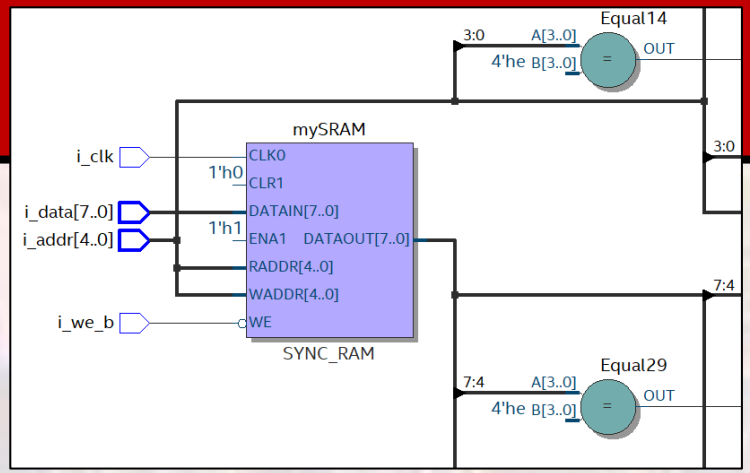
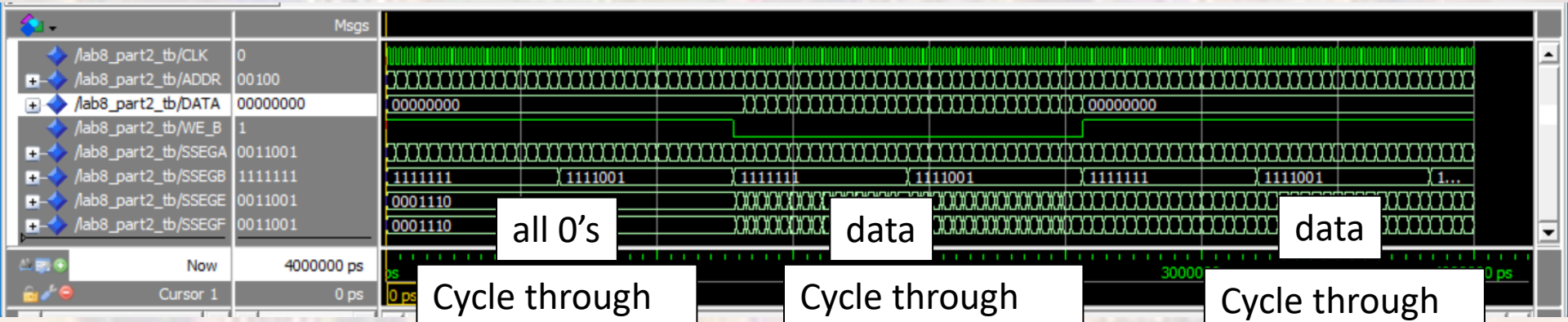
Lab8 – Part2

```
entity lab8_part2 is
    port(
        i_clk:      in    std_logic;
        i_we_b:     in    std_logic;
        i_addr:     in    std_logic_vector(4 downto 0);
        i_data   :  in    std_logic_vector(7 downto 0);

        o_addr_sseg_A: out   std_logic_vector(6 downto 0);
        o_addr_sseg_B: out   std_logic_vector(6 downto 0);
        o_data_sseg_E: out   std_logic_vector(6 downto 0);
        o_data_sseg_F: out   std_logic_vector(6 downto 0)
    );
end;
```





all 0's

Cycle through addresses – no write

data

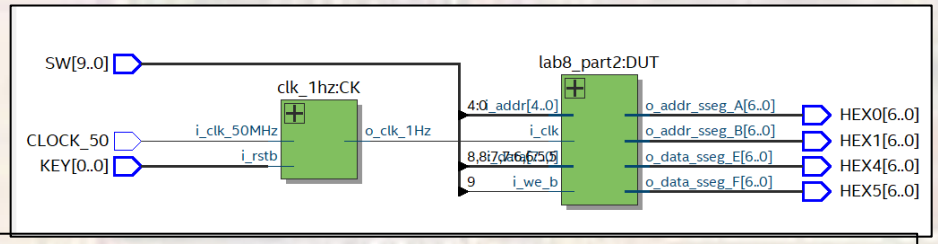
Cycle through addresses – and write data

data

Cycle through addresses – no write

```
entity lab8_part2_de10 is
    port(
        CLOCK_50:   in    std_logic;
        SW:         in    std_logic_vector(9 downto 0);
        KEY:        in    std_logic_vector(0 downto 0);

        HEX0:       out   std_logic_vector(6 downto 0);
        HEX1:       out   std_logic_vector(6 downto 0);
        HEX4:       out   std_logic_vector(6 downto 0);
        HEX5:       out   std_logic_vector(6 downto 0)
    );
end entity;
```



Only 4 data input switches but data is 8 bits wide I doubled up on the input bits b3 b2 b1 b0 to form the data input b3 b3 b2 b2 b1 b1 b0 b0 e.g. if I input 1010, I store 11001100 and read out CC