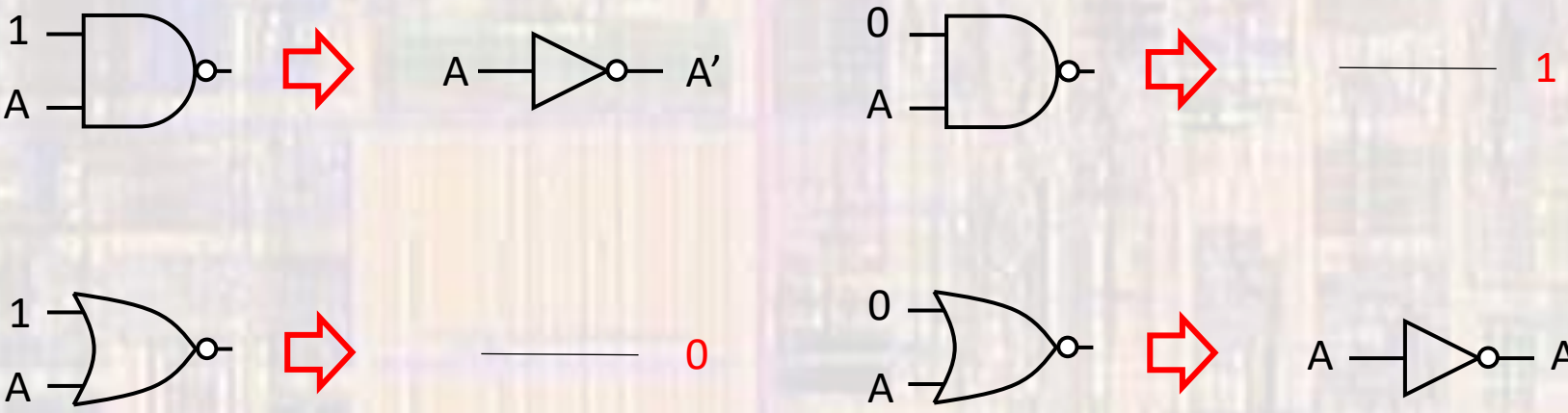
Latches

Last updated 1/11/21

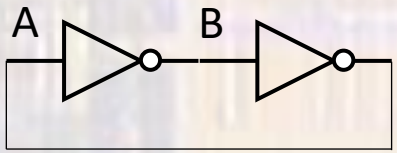
Latches

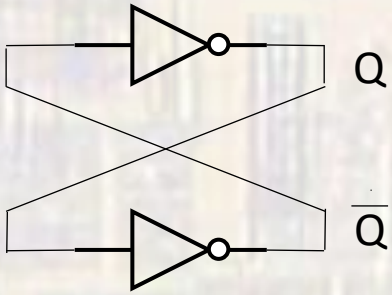
- Shortcuts



Latches

- Bi-stable circuit
  - Circuit with 2 stable operating points
  - Holds 1 element of memory
    - 1 state variable
    - 2 values for the state variable
      - 1 bit – 0 or 1





state variable

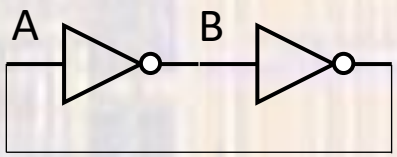
State	A	B
1	0	1
2	1	0

state variable

State	Q	$\overline{Q}$
1	0	1
2	1	0

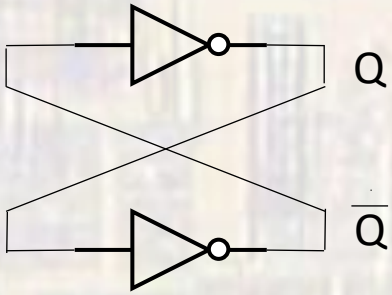
Latches

- Bi-stable circuit
  - Circuit with 2 stable operating points
  - Holds 1 element of memory
    - 1 state variable
    - 1 bit



What's wrong with this circuit

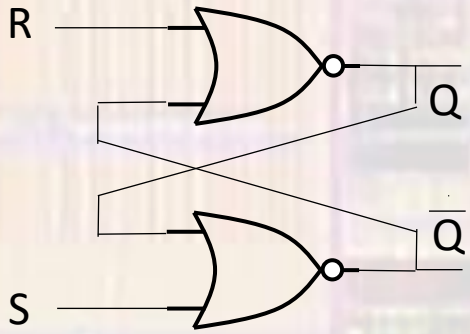
State	A	B
1	0	1
2	1	0



State	Q	$\overline{Q}$
1	0	1
2	1	0

Latches

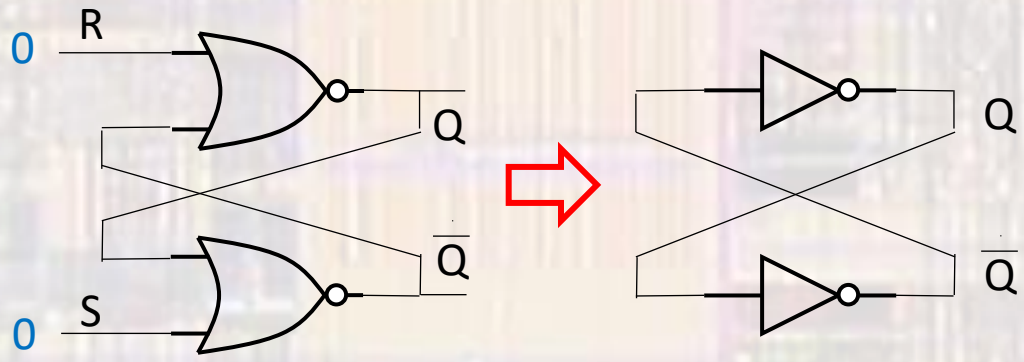
- SR Latch (set/reset)
  - Bi-stable circuit
  - Added ability to set the state



R : Reset
S : Set

Latches

- SR Latch (set/reset)
  - 0,0 Inputs

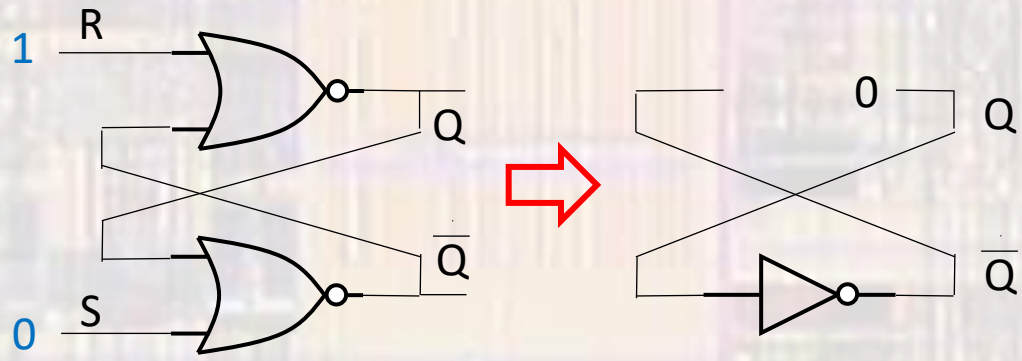


Latch

S	R	Q
0	0	Q_{old}

Latches

- SR Latch (set/reset)
  - 0,1 Inputs

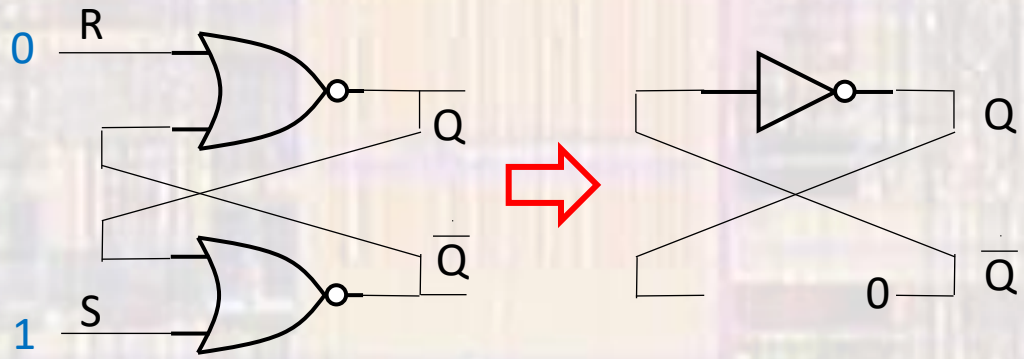


S	R	Q
0	0	Q_{old}
0	1	0

Reset

Latches

- SR Latch (set/reset)
  - 1,0 Inputs

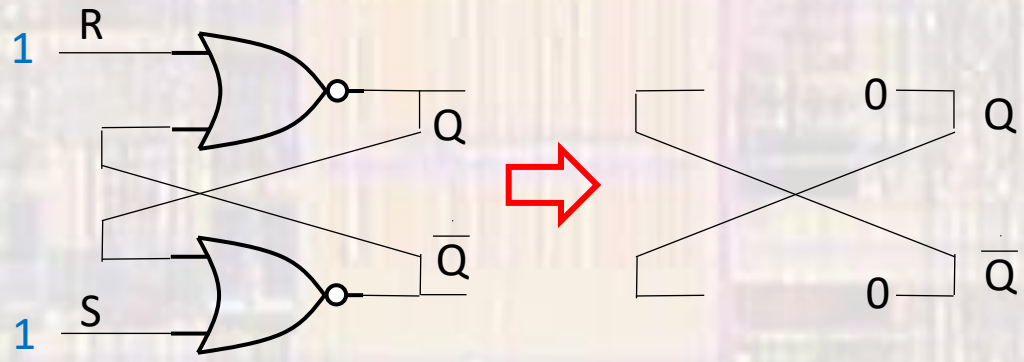


Set

S	R	Q
0	0	Q_{old}
0	1	0
1	0	1

Latches

- SR Latch (set/reset)
  - 1,1 Inputs

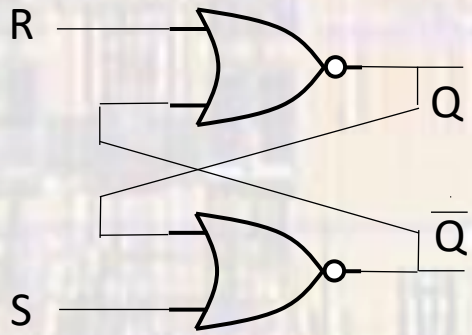


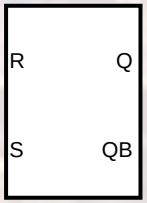
S	R	Q
0	0	Q_{old}
0	1	0
1	0	1
1	1	0

Fault?

Latches

- SR Latch (set/reset)
  - Sequential
    - Output depends on Inputs and 1 state variable Q (Q_{old})
    - Asynchronous – output changes occur when inputs change
    - Memory is in the bi-stable latch

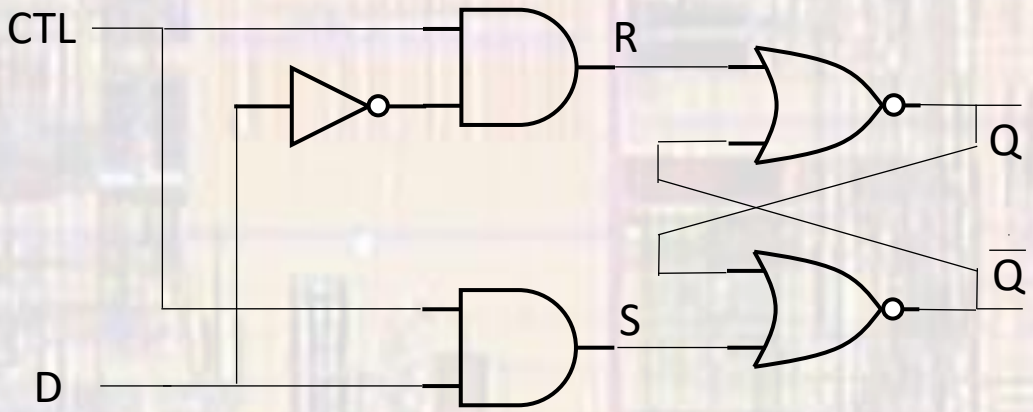




S	R	Q
0	0	Q_{old}
0	1	0
1	0	1
1	1	0

Latches

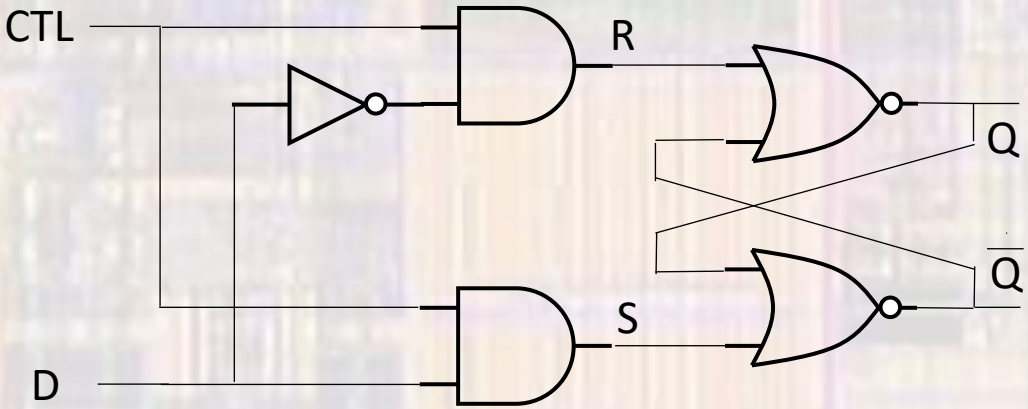
- D Latch (data)
  - Bi-stable circuit
  - Added ability to set the state
  - Output changes limited to specific input conditions

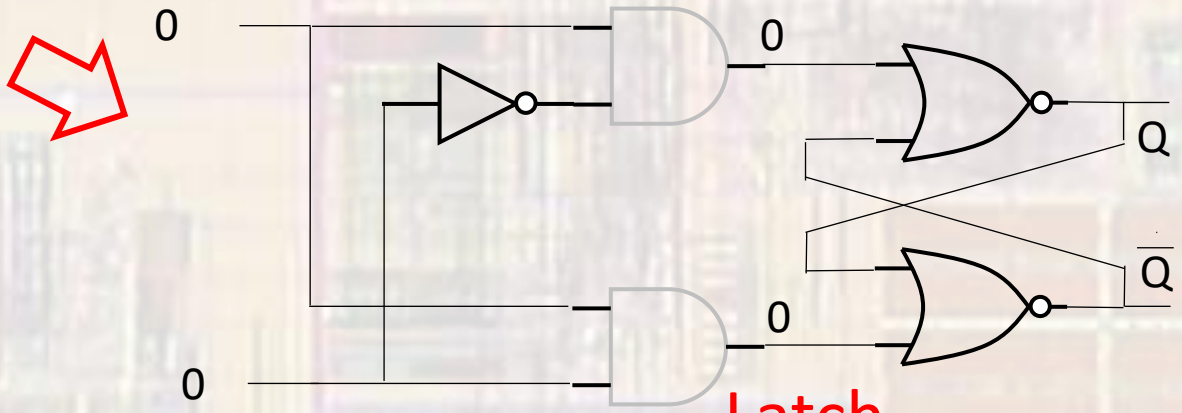


Latches

- D Latch (data)
  - 0,0 inputs – control (CTL), data (D)

CTL	D	Q
0	0	Q_{old}



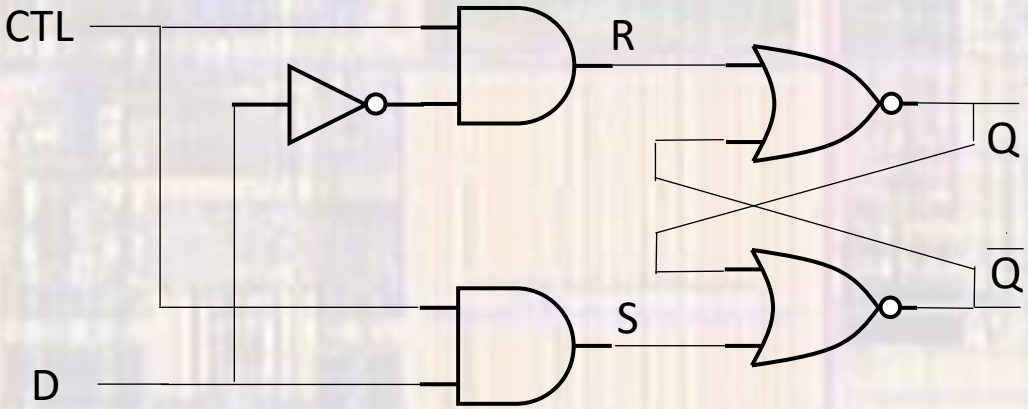


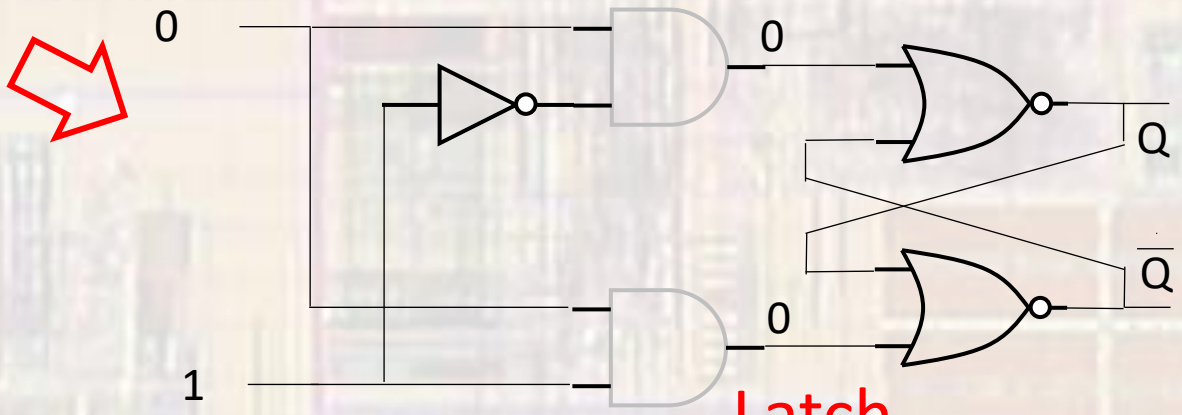
Latch

Latches

- D Latch (data)
  - 0,1 inputs – control, data

CTL	D	Q
0	0	Q_{old}
0	1	Q_{old}

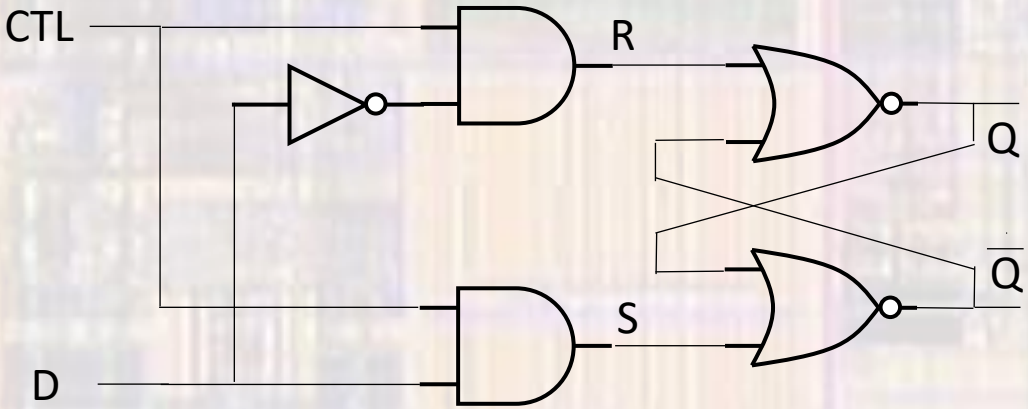




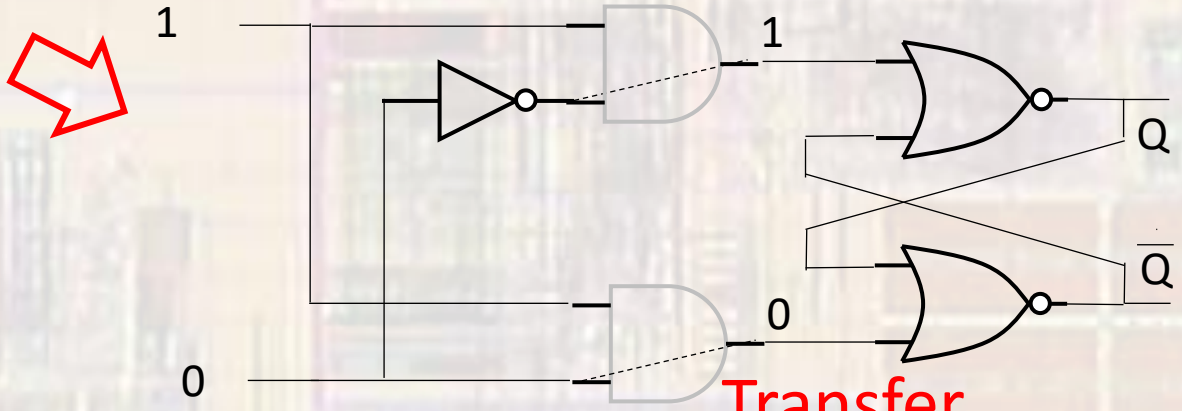
Latch

Latches

- D Latch (data)
  - 1,0 inputs – control, data



CTL	D	Q
0	0	Q_{old}
0	1	Q_{old}
1	0	0 (D)

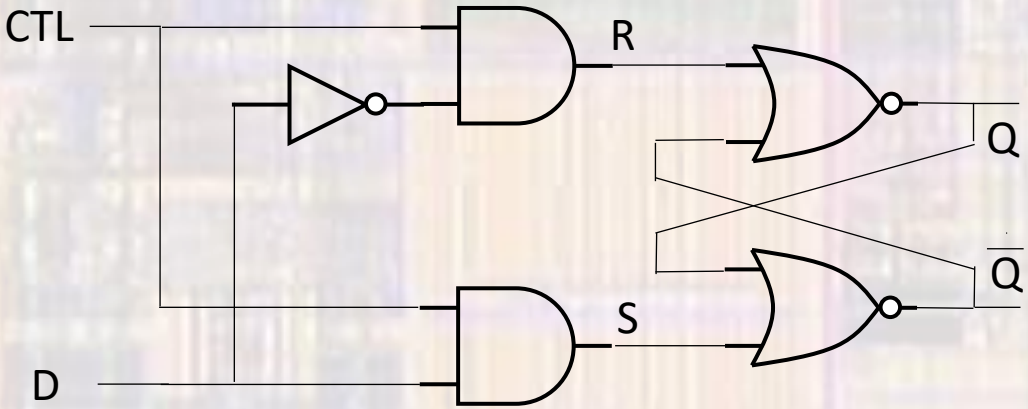


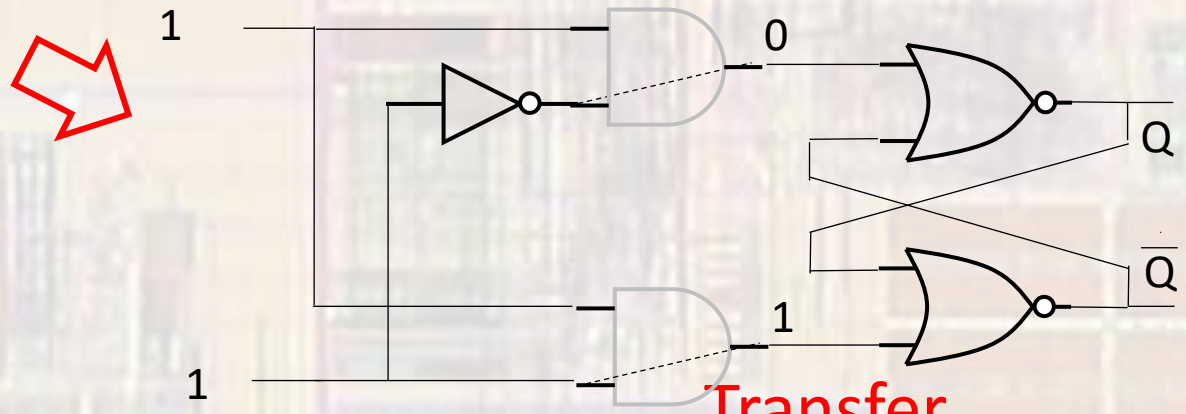
Transfer

Latches

- D Latch (data)
  - 1,1 inputs – control, data

CTL	D	Q
0	0	Q_{old}
0	1	Q_{old}
1	0	0 (D)
1	1	1 (D)

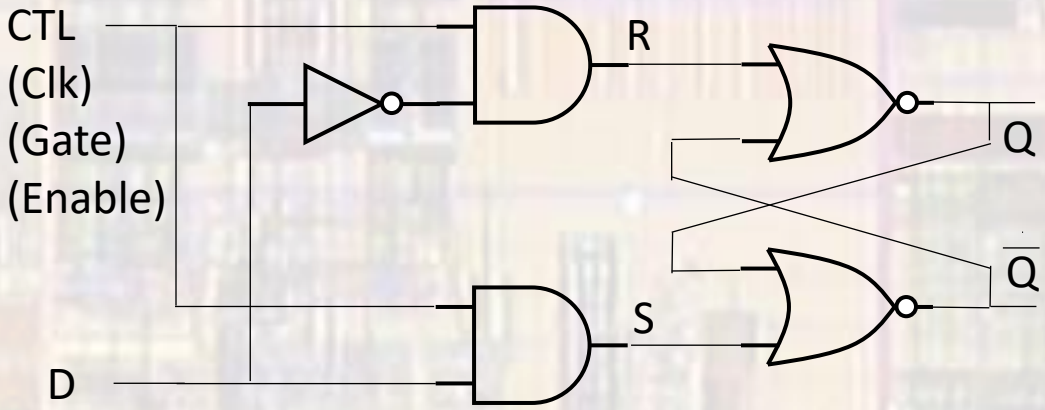


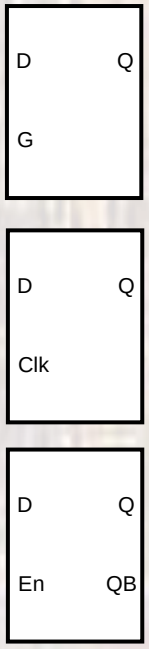


Transfer

Latches

- D Latch (data)
  - Sequential
    - Output depends on Inputs and 1 state variable (Q)
    - Asynchronous – output changes occur when inputs change
    - Memory is in the bi-stable latch
    - Control input: Clk(clock), G (gate), En (enable)





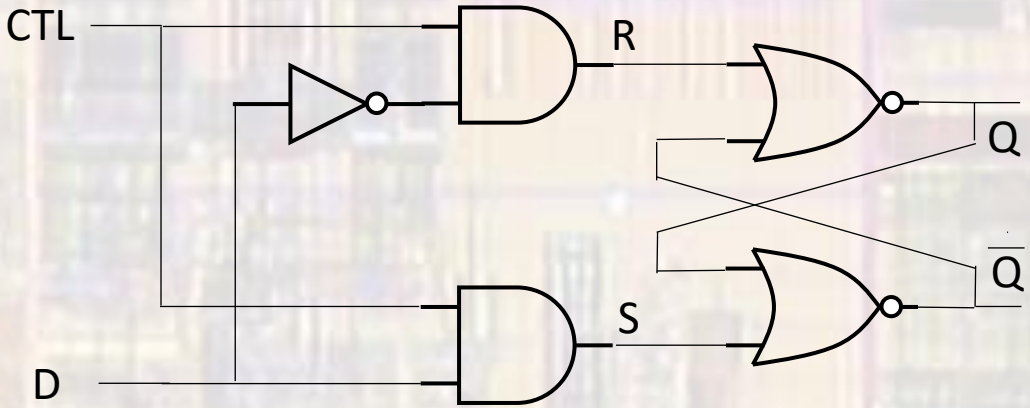
CTL	D	Q
0	x	Q_{old}
1	D	D

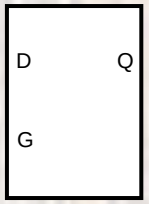
Latches

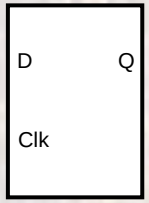
- D Latch (data)

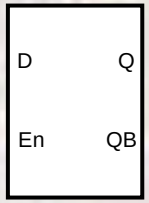
Level Sensitive Latch

CTL = low → latched
CTL = high → Transfer









CTL	D	Q
0	x	Q_{old}
1	D	D