Logic Timing

Last update 1/15/21

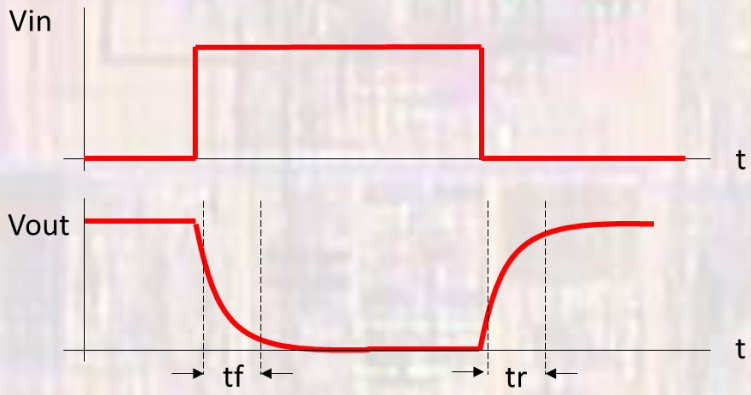
Logic Timing

- Fundamentals
  - AC Characteristics
    - T_{rise} and T_{fall} : 10% - 90 %

$Vout = V_{DD}(e^{-t/RC})$ $Vout = V_{DD}(1 - e^{-t/RC})$

Logic Timing

- Fundamentals
  - AC Characteristics
    - Vout = $V_{DD}(e^{-t/RC})$
    - Vout = $V_{DD}(1 - e^{-t/RC})$

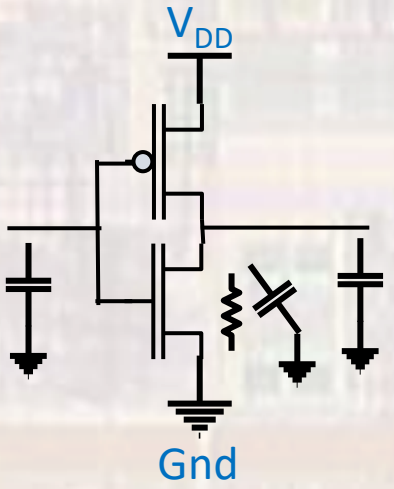


- R

the internal equivalent resistance of the N_{MOS} or P_{MOS} devices

+

the distributed resistance of the wires (negligible for our purpose)



- C

is the internal capacitance of the N_{MOS} and P_{MOS} Drains (C_{DRAIN})

+

the Gate capacitance of any logic gates being driven

+

the capacitance of any connecting wires

} (C_{LOAD})

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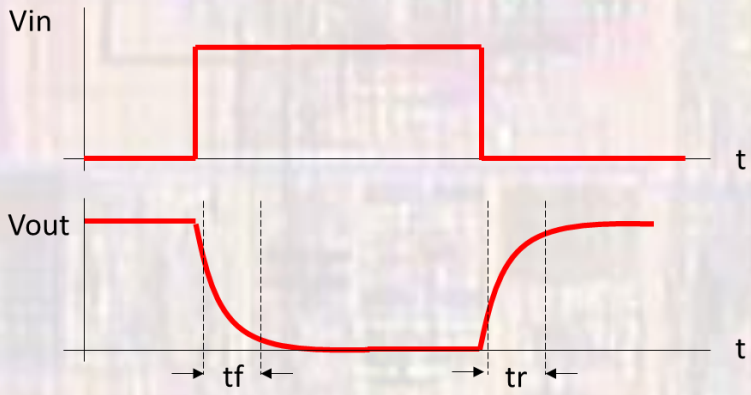
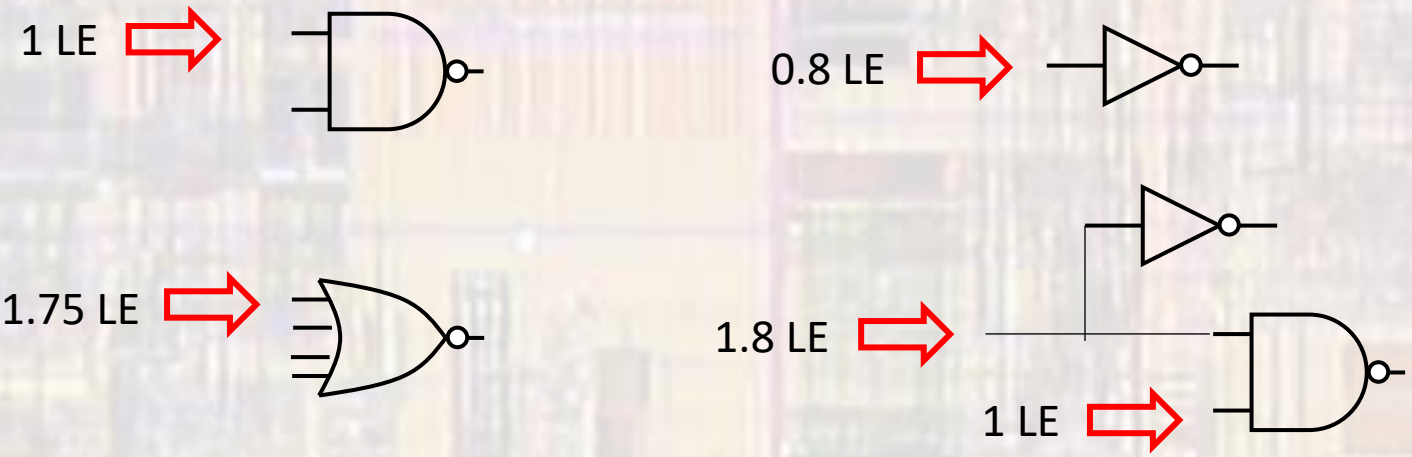


  - R and C_{DRAIN} are gate design dependent and known
    - Fixed for any given gate
  - C_{LOAD} = capacitance of driven gates + interconnect
    - Circuit dependent

Logic Timing

- Gate level timing
  - Each gate **input** has an equivalent input load factor
    - Models the input capacitance
    - Load equivalent (LE)
    - Technology / Process dependent

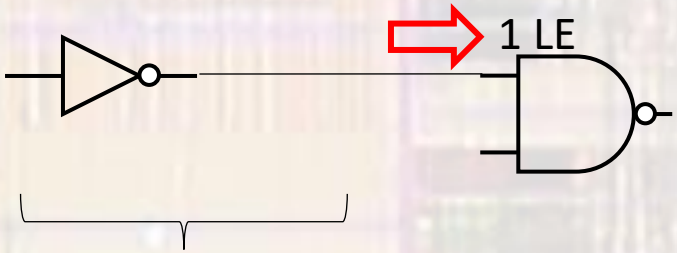


Logic Timing

- Gate level timing
  - Each gate has internal delay
    - Assumes a fixed external load – 1 LE
    - Circuit dependent – but fixed
    - Technology / Process dependent

Logic Timing

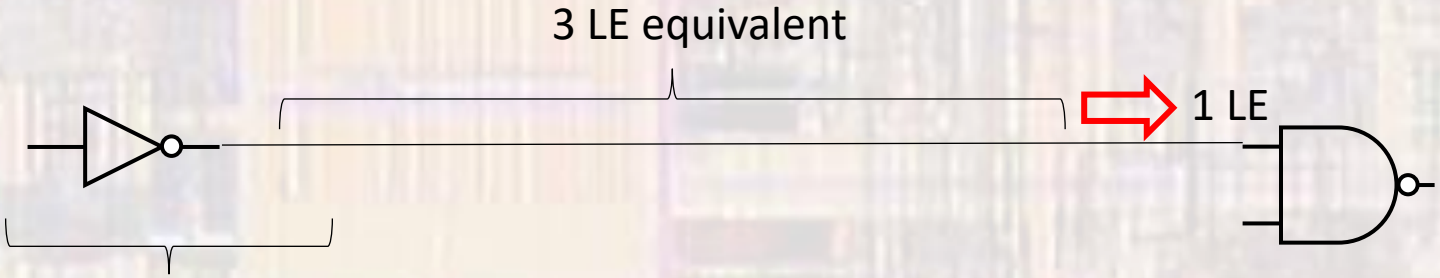
- Gate level timing
  - Each gate has a variable delay factor - r
    - Function of the gate's drive capability
    - Modifies the circuit delay based on the amount of loading
    - Circuit dependent



$$t_{pd_{inv}} + r \times 1\ LE$$

Logic Timing

- Gate level timing
  - Long wires have enough capacitance to impact delays
    - Model long wires in terms of load equivalents (LEs)
    - Modifies the circuit delay based on the amount of loading
    - Circuit dependent



$$t_{pd_{inv}} + r \times (3\ LE + 1\ LE)$$

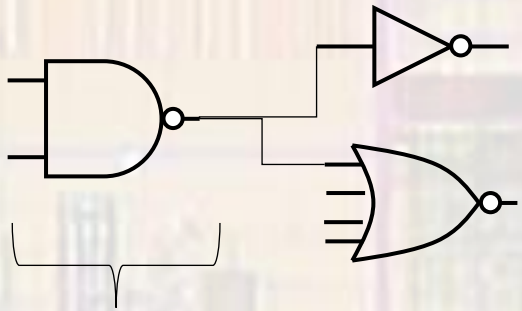
Digital Circuit Timing

- Gate level timing

$t_{pd} = t_{fixed\_delay} + r_{variable\_delay\_factor} * \text{Load Equivalents}$

Standard

Gate	INV	2-NAND	2-NOR	4-NAND	4-NOR
Input load factor	0.8	1.0	1.0	1.75	1.75
Fixed delay factor	50ps	65ps	65ps	80ps	80ps
Variable delay factor (r)	5ps/LE	8ps/LE	8ps/LE	12ps/LE	12ps/LE



$t_{pd} = 65ps + 8ps/LE*(0.8LE + 1.75LE) = 84.5ps^{**}$

** we are assuming interconnect capacitance is negligible

Digital Circuit Timing

- Gate level timing

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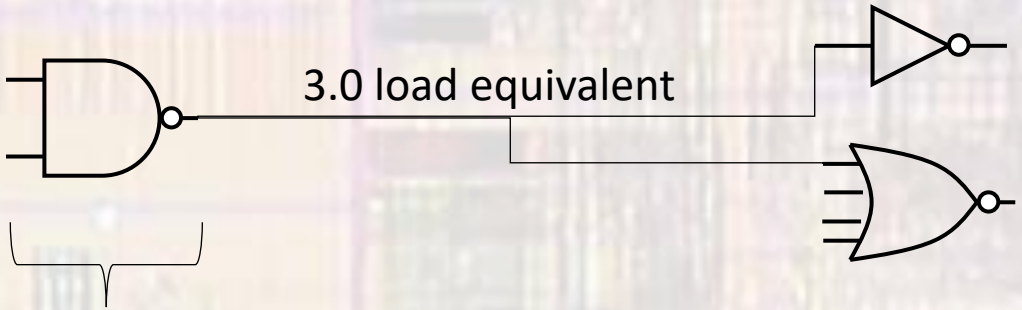

$t_{pd} = 65ps + 8ps/LE*(0.8LE + 1.75LE + 3.0LE) = 109.4ps$

