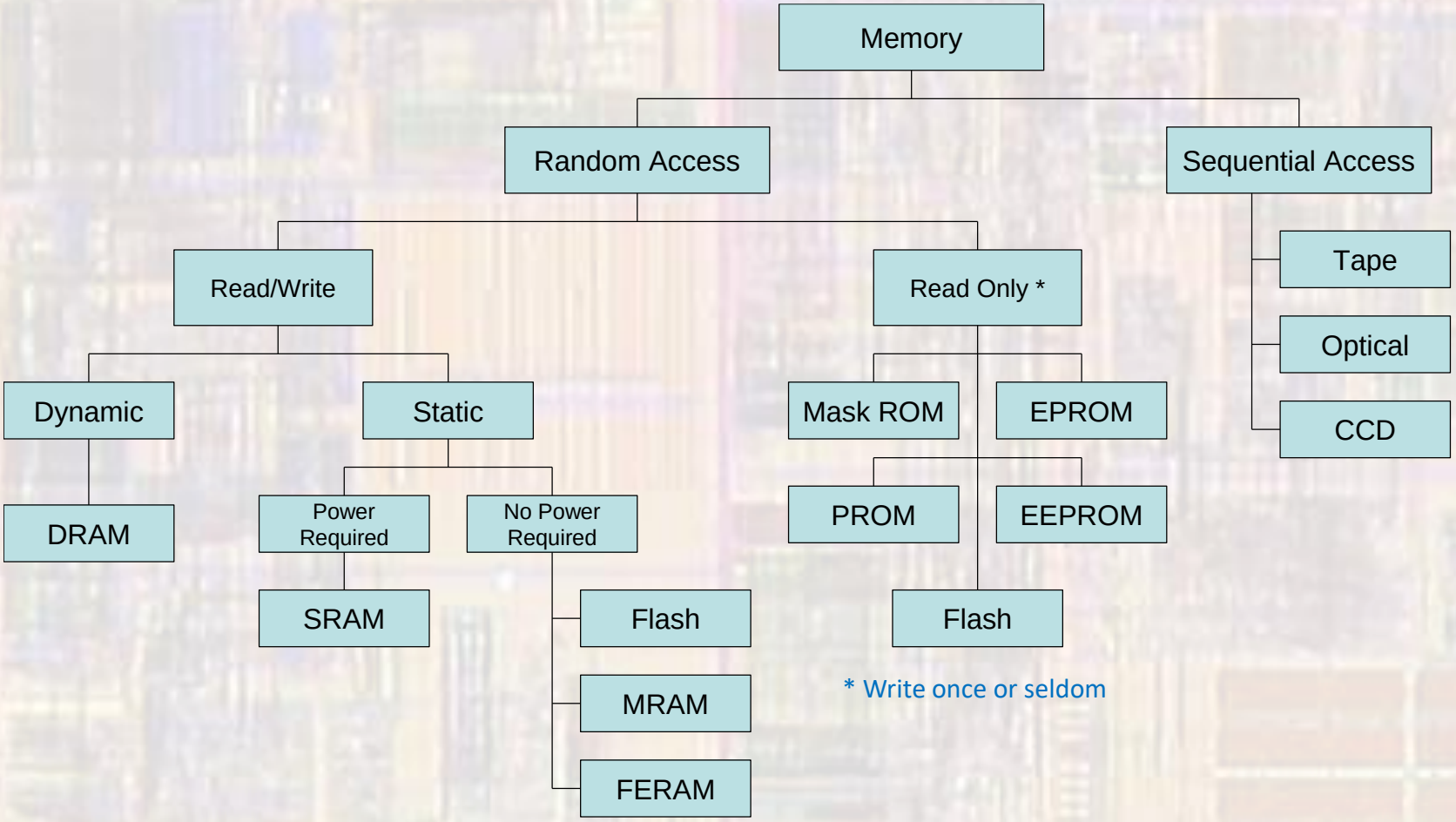
Memory Intro

Last updated 1/25/21

Memory Intro

- Memory Taxonomy



Memory Intro

- Memory Taxonomy
  - Key Attributes
    - Sequential vs. Random Access
      - Sequential – must traverse the memory to the location you want
        - Audio cassette tape
      - Random Access – can directly access the location you want
        - Track selection on a CD/DVD
    - Read only vs. Read/Write
      - Read only – data stored permanently in the memory
        - Commercial Blu-ray
      - Read/Write – data can be modified
        - DVD – R/W

Memory Intro

- Memory Taxonomy
  - Key Attributes – cont'd
    - Static vs. Dynamic
      - Static – retains it's value as long as power is supplied
        - Current location in a paused video
      - Dynamic – looses it's value over time if nothing is done to protect it even though power is applied
        - Air in a soccer ball (with a pump attached but not operating)
    - Volatile vs. non-Volatile
      - Volatile – looses it's value when power is removed
        - Current location in a paused video
      - Non-volatile – retains it's value even when no power is supplied
        - Thumb drive

Memory Intro

- Memory Taxonomy
  - Key Measures
    - Density
      - amount of storage space
    - Speed
      - Read or Write speed
      - Can be different for first access vs. follow on accesses
    - Power
      - Static – powered up but not doing anything
      - Dynamic – reading or writing
    - Cost / bit

Memory Intro

- Memory Taxonomy
  - Terminology WARNING – WARNING - WARNING
  - b – bit
  - B – Byte

Memory Intro

- Memory Taxonomy
  - Terminology WARNING – WARNING - WARNING
  - K, M, G, T have special meaning in digital technology
    - sometimes replaced with Ki, Mi, Gi, Ti
  - 1Mb can mean either 1,048,576 bits
    or 1,000,000 bits

Binary					
Value		IEC		JEDEC	
1024	2^{10}	Kibit	**kibibit**	Kbit	kilobit
1024^2	2^{20}	Mibit	mebibit	Mbit	megabit
1024^3	2^{30}	Gibit	gibibit	Gbit	gigabit
1024^4	2^{40}	Tibit	tebibit		-
1024^5	2^{50}	Pibit	pebibit		-
1024^6	2^{60}	Eibit	exbibit		-
1024^7	2^{70}	Zibit	zebibit		-
1024^8	2^{80}	Yibit	yobibit		-
src: wikipedia					

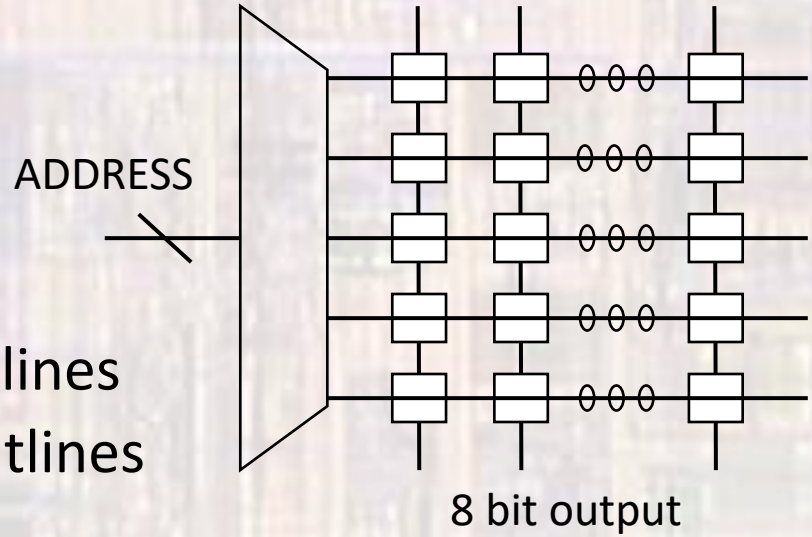
You must determine the meaning in any given situation

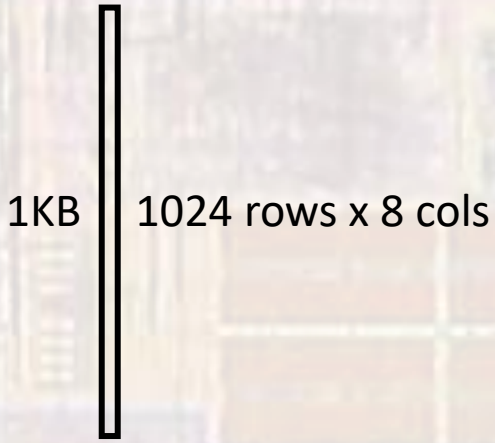
Memory Intro

- Memory Taxonomy
  - Terminology WARNING – WARNING - WARNING
  - 16Gb Flash drive when checked on your PC may read 14.9Gb

Memory Intro

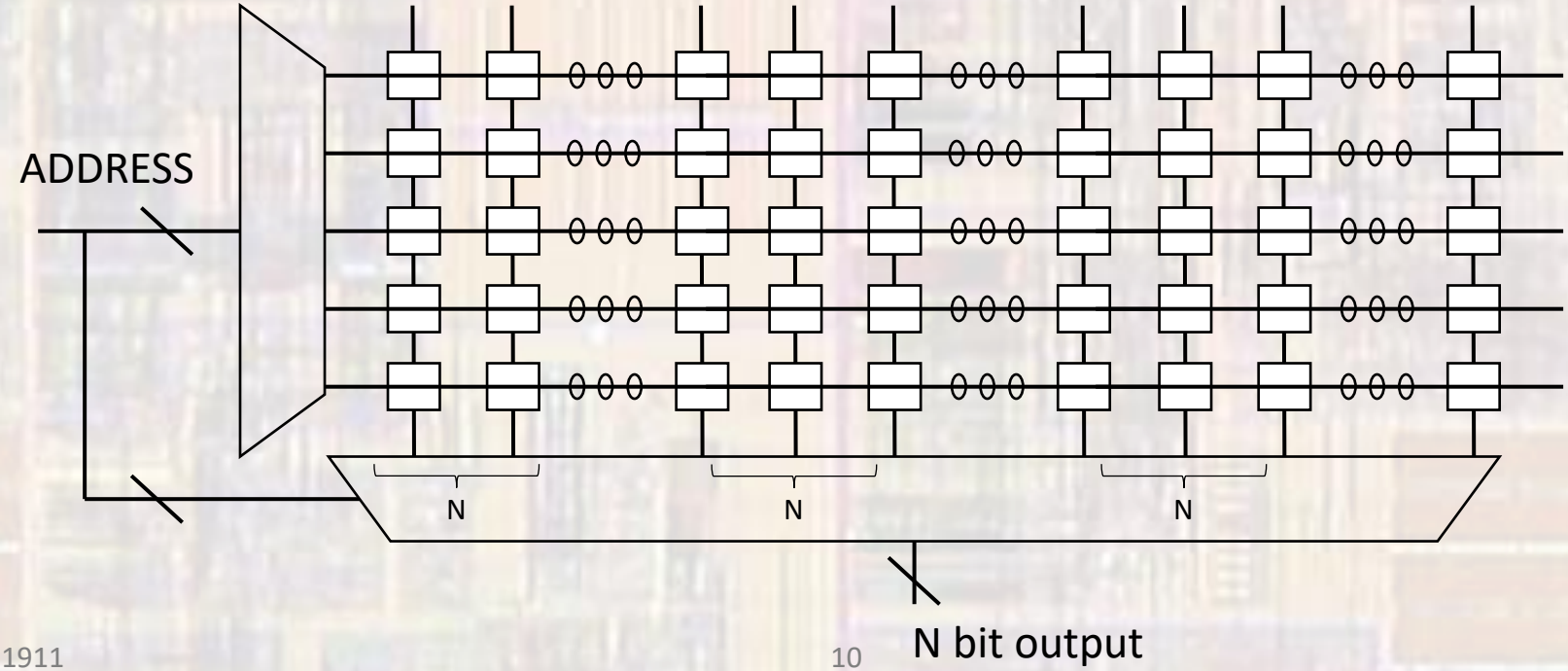
- Basic Memory Topology
  - Array of single bit cells
  - Row decoder chooses 1 row
  - Rows are typically called wordlines
  - Columns are typically called bitlines
  - Non optimal
    - Physical implementation
      - Array
      - Decoder
    - Speed
      - Column capacitance very large





Memory Intro

- General Memory Topology
  - Array of n bit cells
  - Row decoder chooses 1 row
  - Column decoder chooses one N bit column
    - 1,4,8,16,32,64,128,… bits/column



Memory Intro

- General Memory Topology
  - Example
  - 16Mb memory in a x4 configuration

x4 means each column is 4 bits

or each address points to 4 bits

16Mb → 16,777,216 bits

16Mb in a x4 configuration → 4 bits / address → 4,194,304 - individual addresses

4,194,304 addresses → 22 address bits

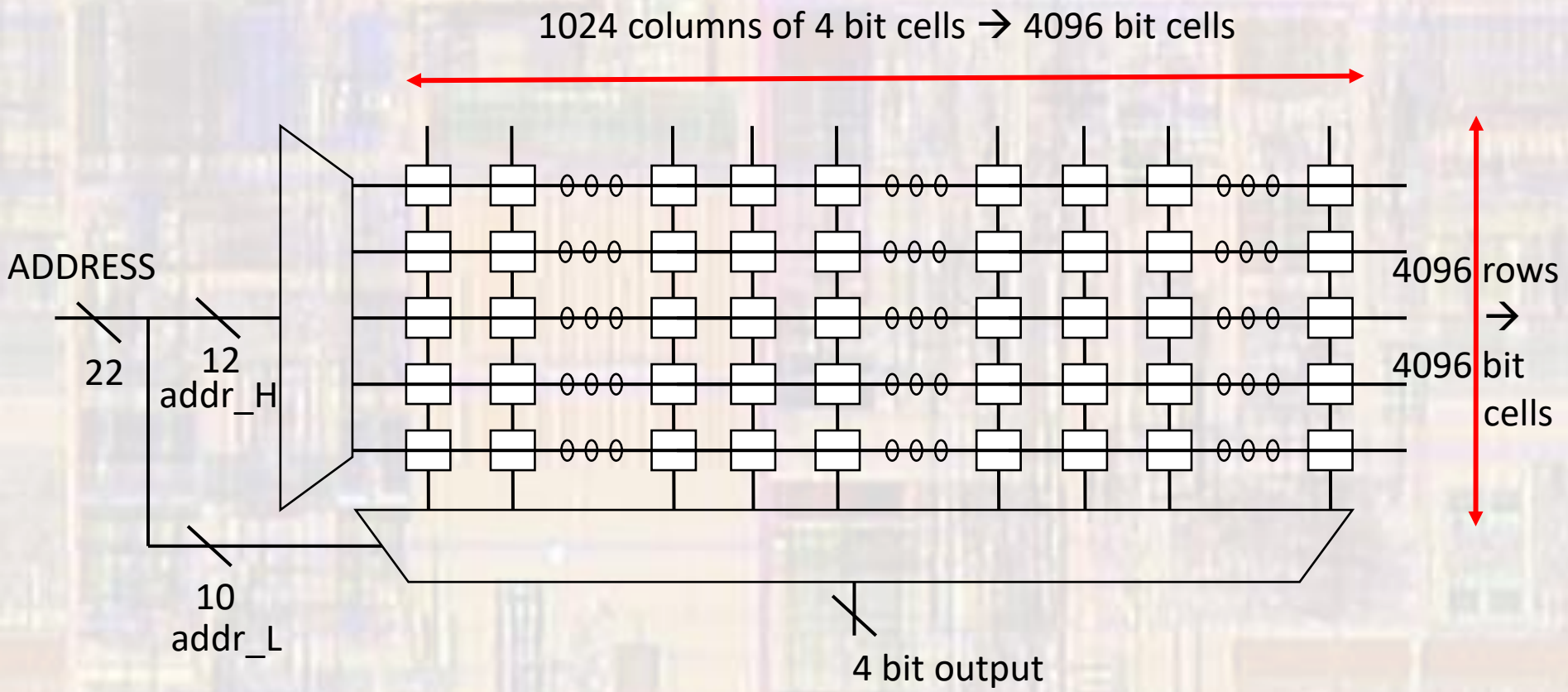
x4 means 4 bit cells for every column

Assuming a square memory array and a square bit cell → 4 times as many rows as columns

22 address bits → 12 bits of row address and 10 bits of column address

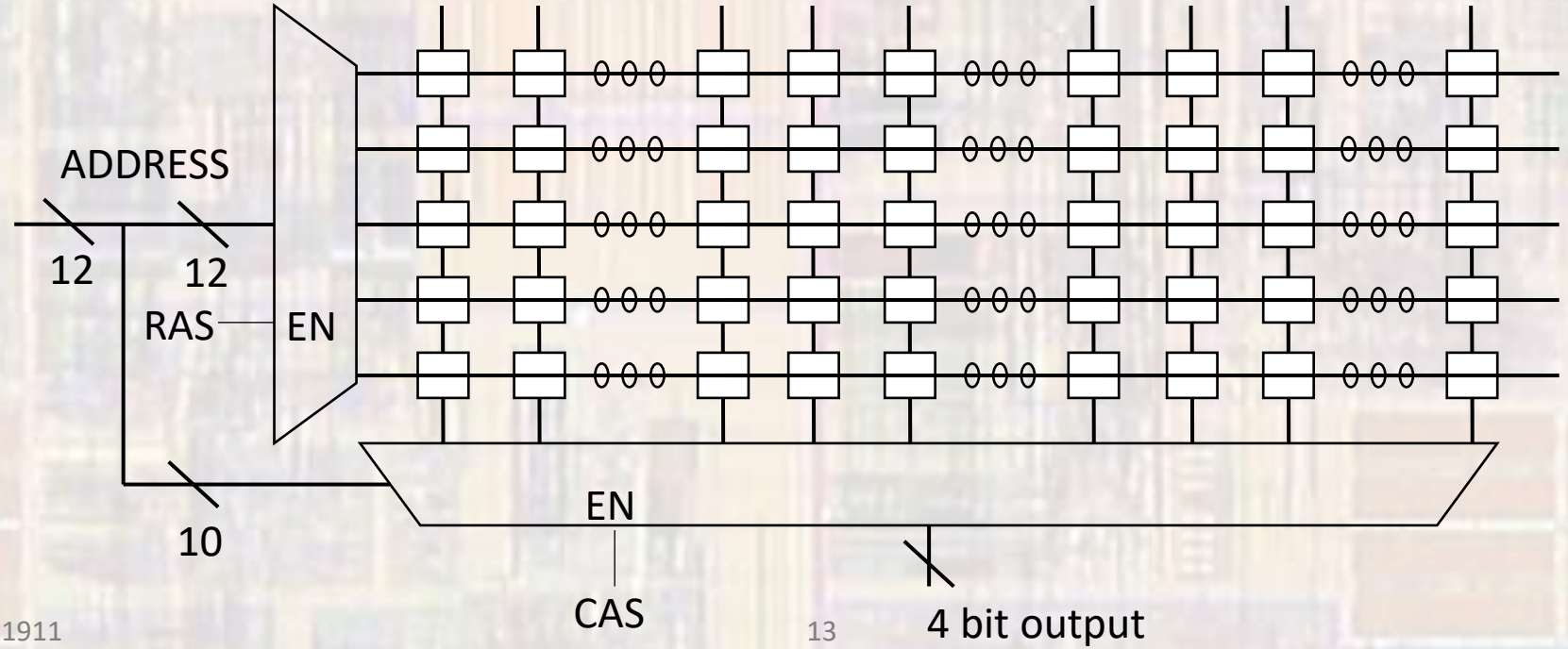
Memory Intro

- General Memory Topology



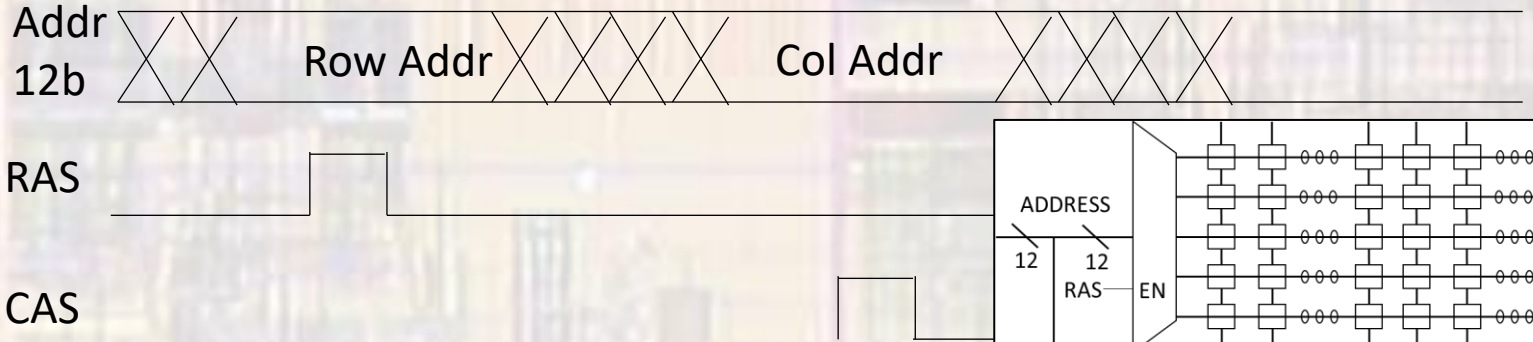
Memory Intro

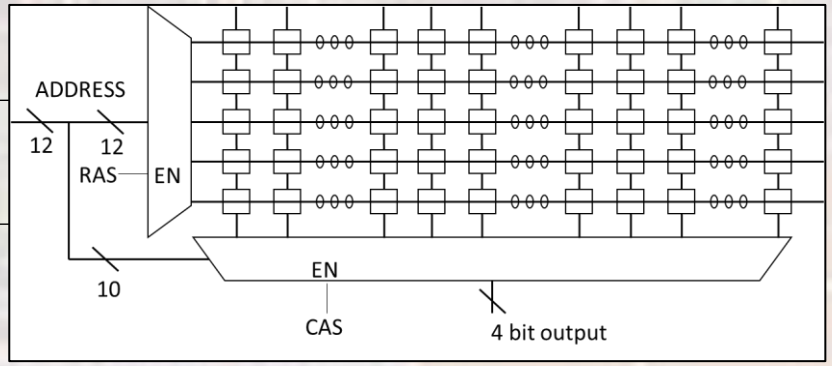
- General Memory Topology
  - Reduce I/O by sharing the address inputs between Row addresses and Column addresses
  - 22 bit addr → 12 bit addr + RAS and CAS → 14 wires
  - RAS – Row Address Strobe (current address is for row decode)
  - CAS – Column Address Strobe (current address is for column decode)



Memory Intro

- General Memory Topology
  - Reduce I/O by sharing the address inputs between Row addresses and Column addresses
  - 22 bit addr → 12 bit addr + RAS and CAS → 14 wires
  - RAS – Row Address Strobe (current address is for row decode)
  - CAS – Column Address Strobe (current address is for column decode)





Memory Intro

- Performance Issues
  - Can 1 bad array element ruin an entire part?
  - Use redundant rows and columns in the array
    - Any bad cells are programmed out at final test
  - Some Memory Management Units (MMUs) can detect poorly performing calls and modify the virtual to physical address translation to remove them from the memory map