Memory - SDRAM

Last updated 1/25/21

Memory - SDRAM

- Dynamic Random Access Memory – DRAM
- Synchronous DRAM - SDRAM
  - Key Attributes
    - Sequential vs. Random Access
    - Read only vs. Read/Write
    - Static vs. Dynamic
    - Volatile vs. non-Volatile
  - Key Measures
    - Density +
    - Speed
    - Power
    - Cost / bit +

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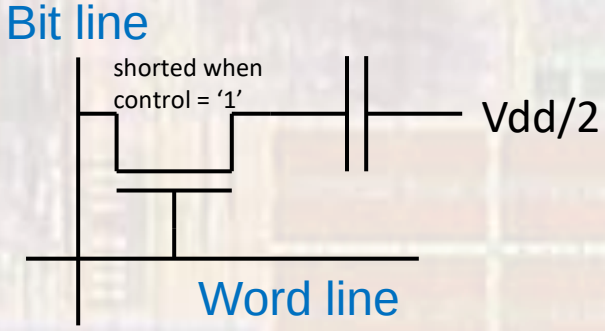
Memory - SDRAM

- DRAM/SDRAM – Synchronous Dynamic Random Access Memory
  - Memory cell (1 bit) is based on capacitor charge storage
  - Bit value decays over time
    - must be recharged – called a refresh cycle
  - Standard SDRAM transfers 1 word each array access
    - DDR – double data rate – transfers 2 words each array access
    - DDR2, DDR3, DDR4 – transfer 4,8,16 words each array access
  - Medium speed
  - Highest density
  - Used as main memory



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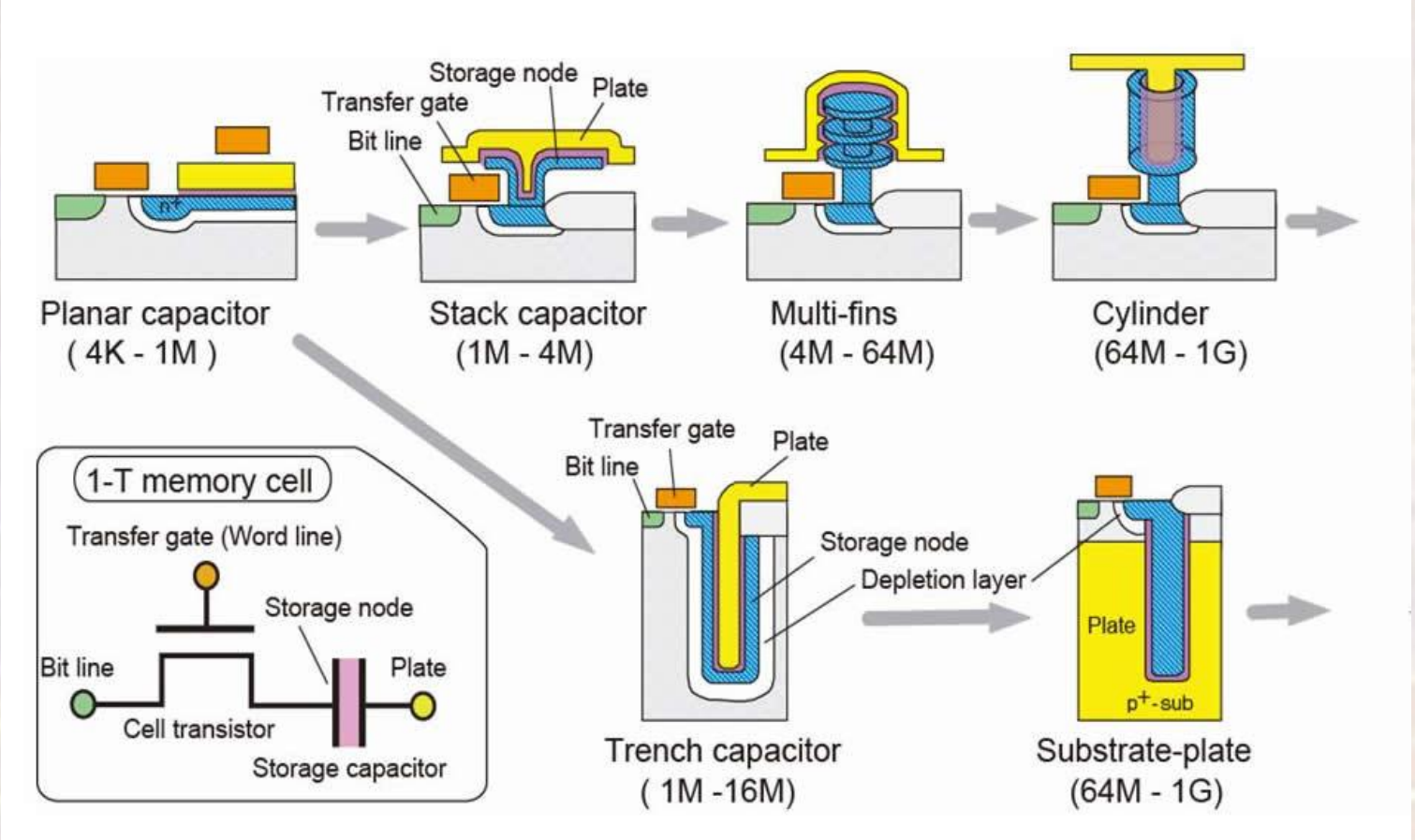
Memory - SDRAM

- SDRAM – Cell



Src: IEDM

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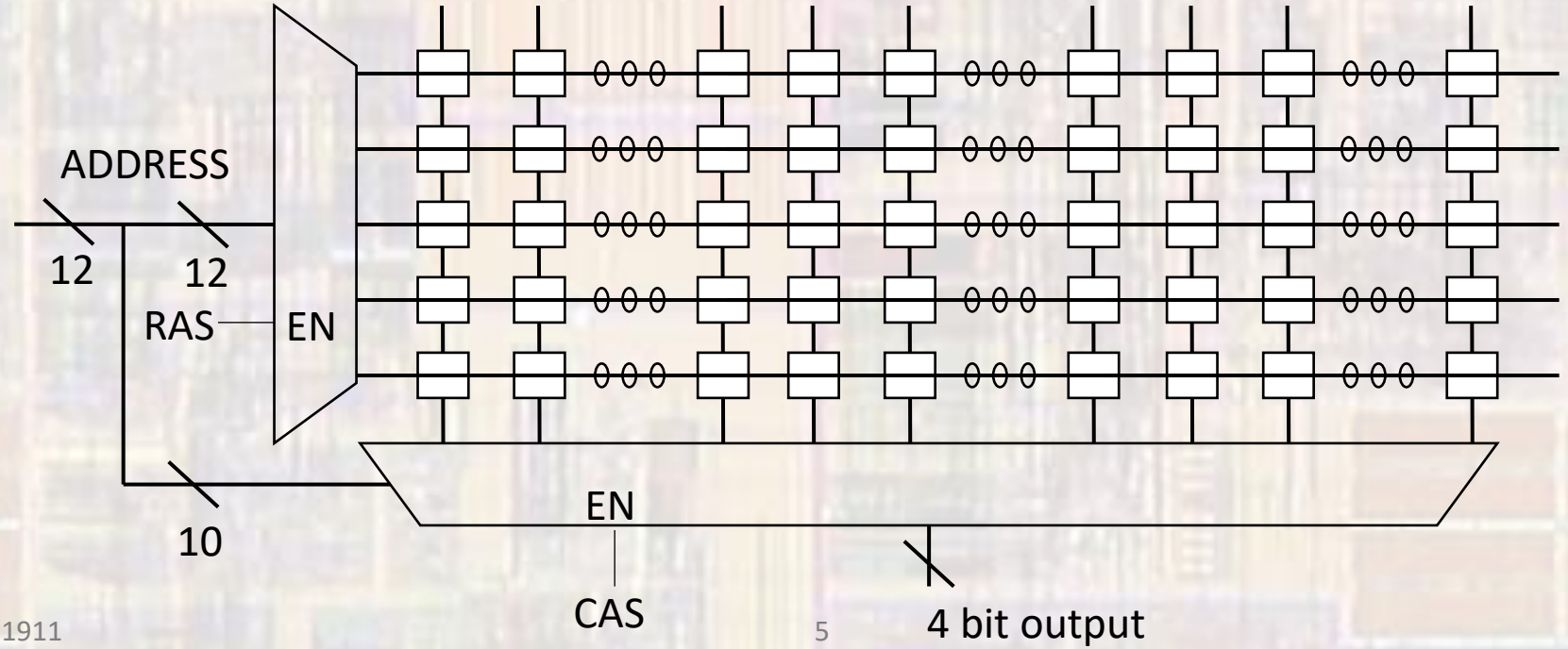
Memory - SDRAM

- General Memory Topology
  - Reduce I/O by sharing the address inputs between Row addresses and Column addresses
  - 22 bit address → 12 bit address + RAS and CAS
  - RAS – Row Address Strobe (current address is for row decode)
  - CAS – Column Address Strobe (current address is for column decode)



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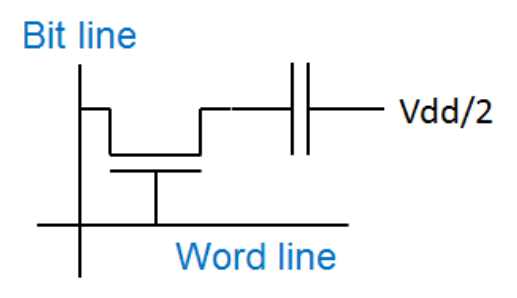
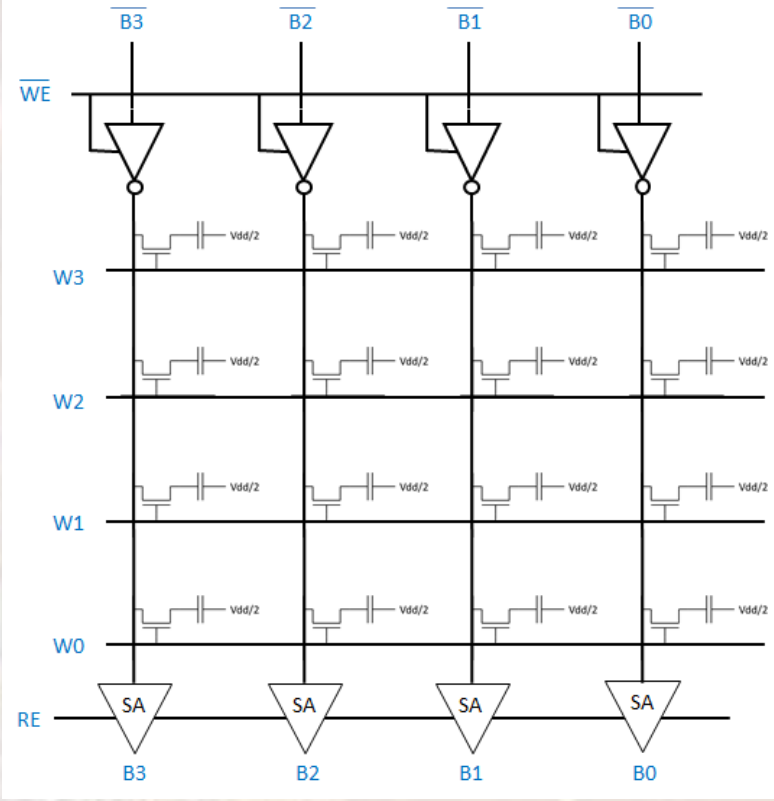
Memory - SDRAM

- Write
  - Read Enable (RE) disabled (low)
  - Place $\overline{B0}$, $\overline{B1}$, $\overline{B2}$, $\overline{B3}$ on inputs (data in)
  - Apply Address (RAS then CAS)
    - Select the desired word line (high)
    - Select the desired column to input to
  - Strobe (clk) write enable bar (WE) low
  - Bit lines write to the bit cell capacitors



4 bits of 1 column



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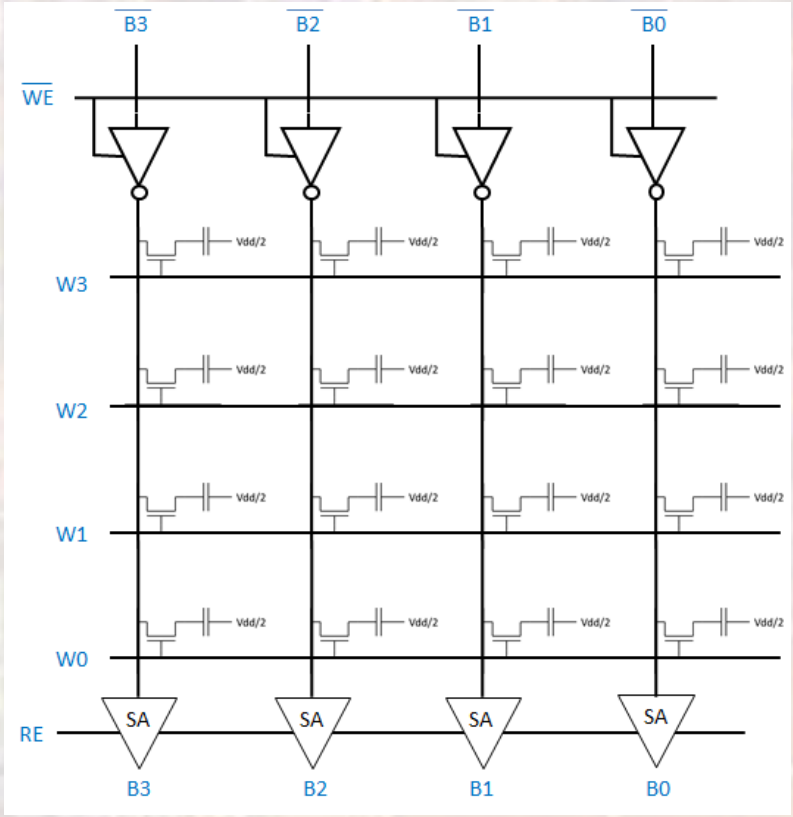
Memory - SDRAM

- Read
  - Write enable bar ($\overline{WE}$) high
    - inverters tristated
  - Read Enable (RE) high
  - Apply Address (RAS then CAS)
    - Select the desired word line (high)
    - Select the desired column to output
  - Sense amplifiers read the value of the capacitors
  - Clk to output the value

  - The read process is destructive !
    - WHY?

4 bits of 1 column



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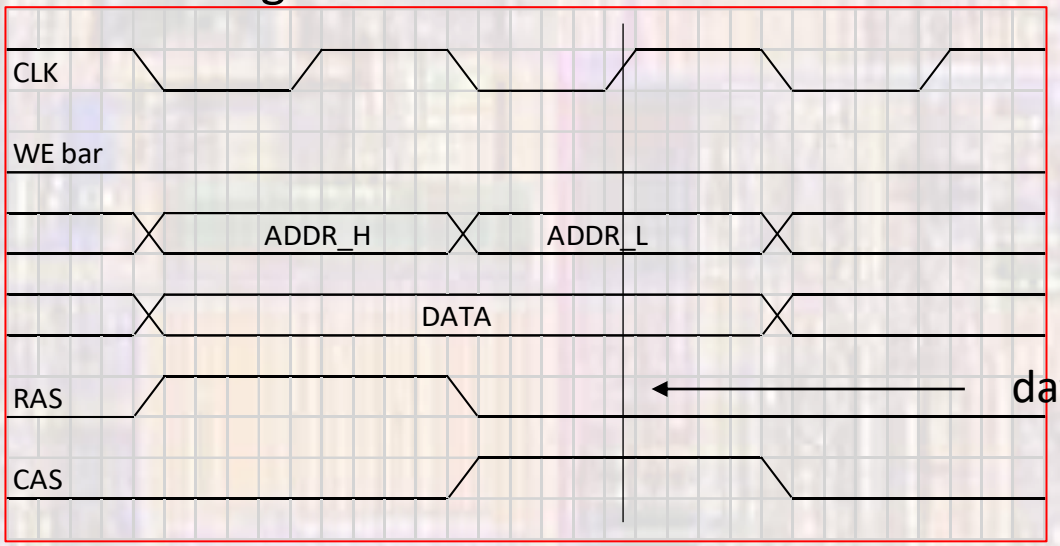
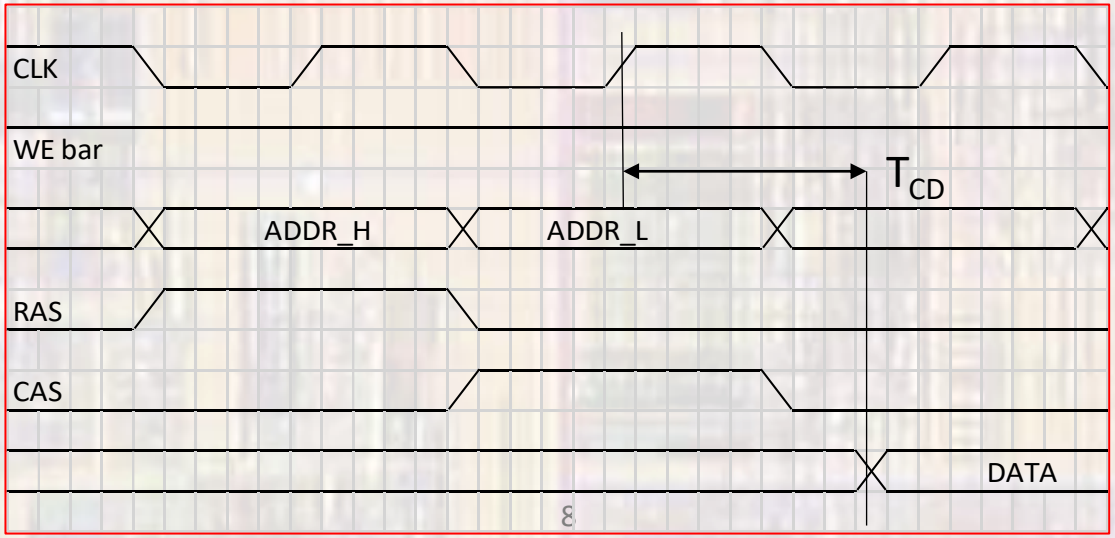
- SDRAM – Timing

WRITE



READ



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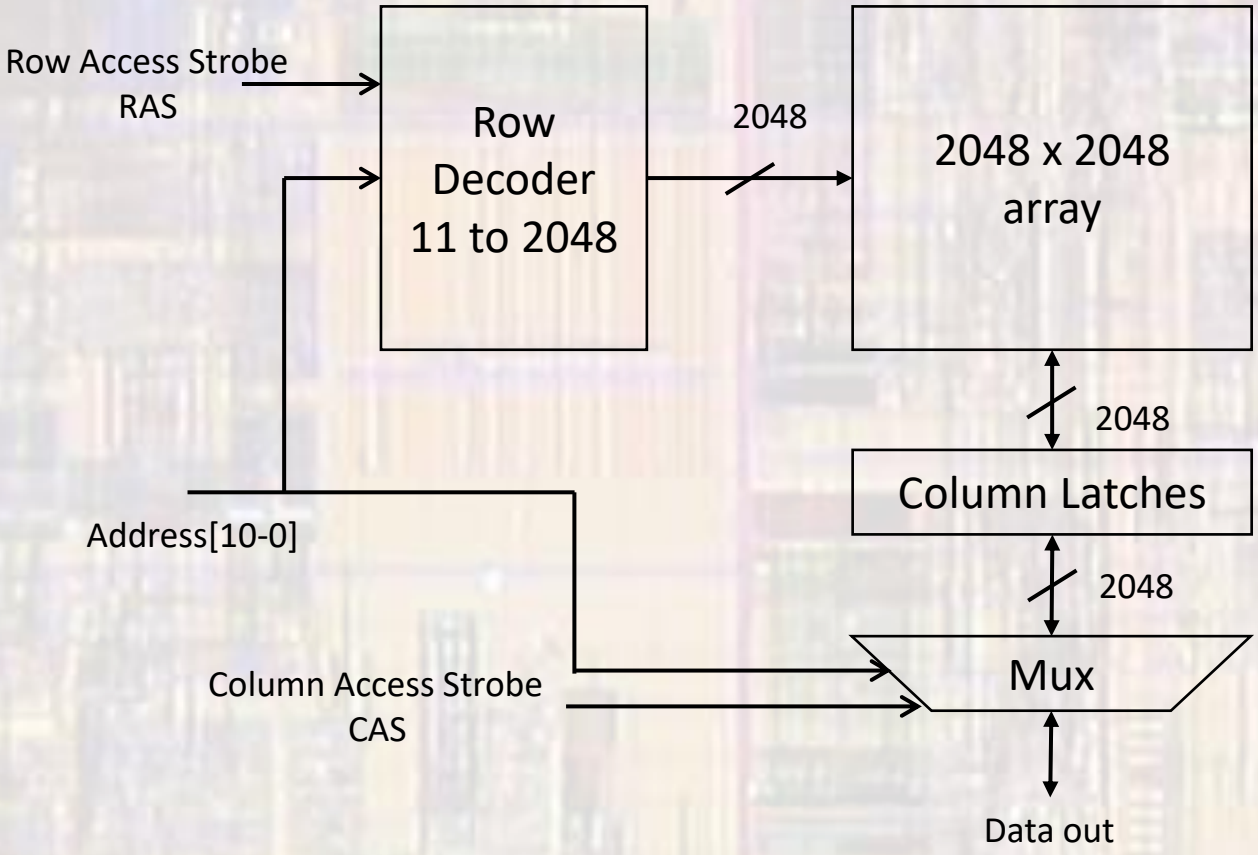
Memory - SDRAM

- SDRAM – Complex Configuration
  - 4Mb in a x1 configuration



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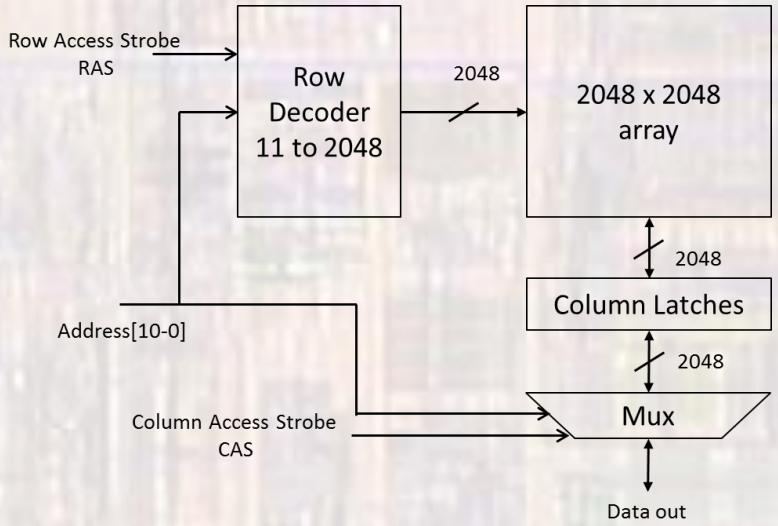
Memory - SDRAM

- SDRAM – Complex Configuration
  - Random Access
  - 4M bits → 22 address bits
  - Operation
    - Place upper 11 bits on address bus
    - Strobe RAS
      - 2048 bits are latched
    - Place lower 11 bits on address bus
    - Strobe CAS
      - Selected bit is fed out



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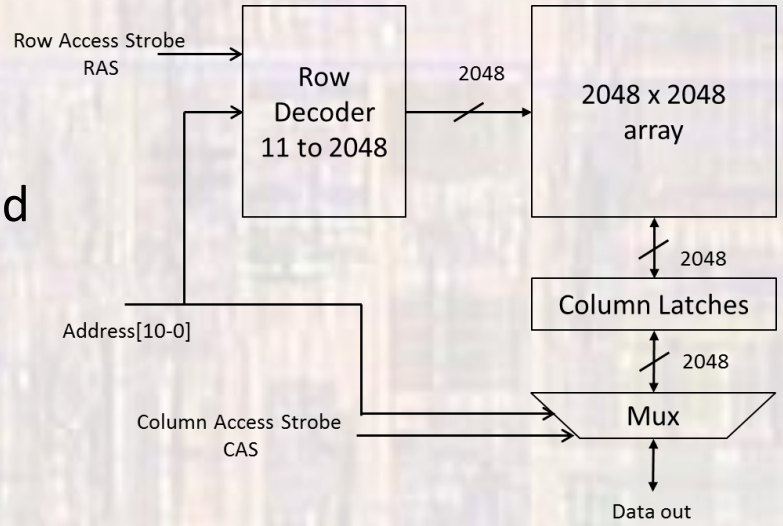
Memory - SDRAM

- Refresh
  - Operation
    - Controller selects a row address - Read
      - 2048 bits are latched
    - The read circuit also re-writes the DRAM cells at the same time



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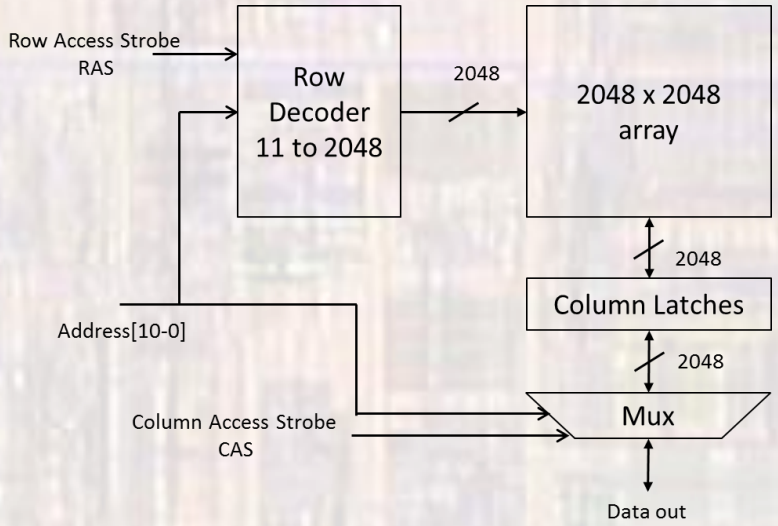
Memory - SDRAM

- Burst Operation
  - 4M bits → 22 address bits
  - Operation
    - Place upper 11 bits on address bus
    - Strobe RAS
      - 2048 bits are latched
    - Place lower 11 bits on address bus
    - Strobe CAS
      - Selected bit is fed out
    - On-chip - Automatically Increment address latch
    - Next clock
      - Next bit is fed out
    - …



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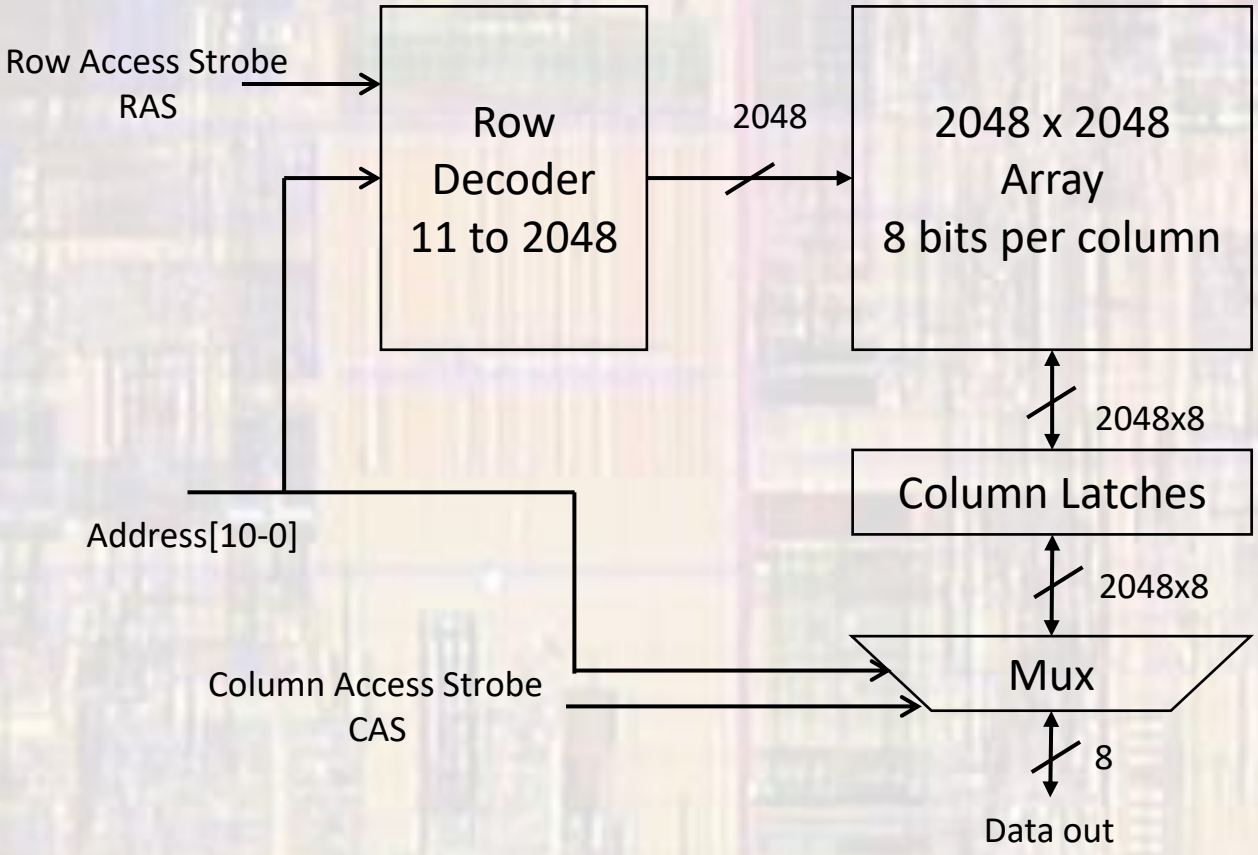
Memory - SDRAM

- Array Layout – 4M X 8 DRAM



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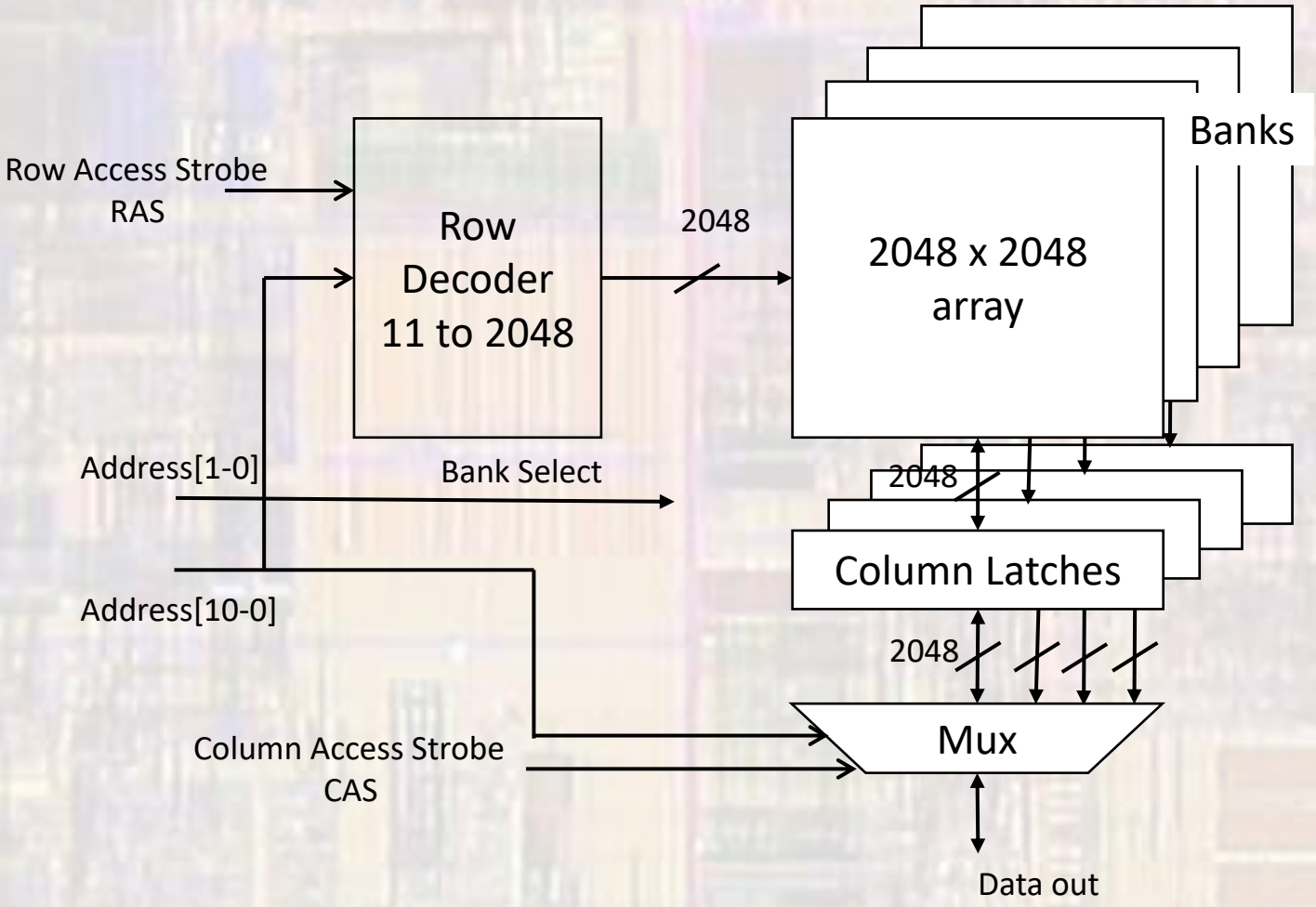
- Array Layout – 16M X 1 DRAM



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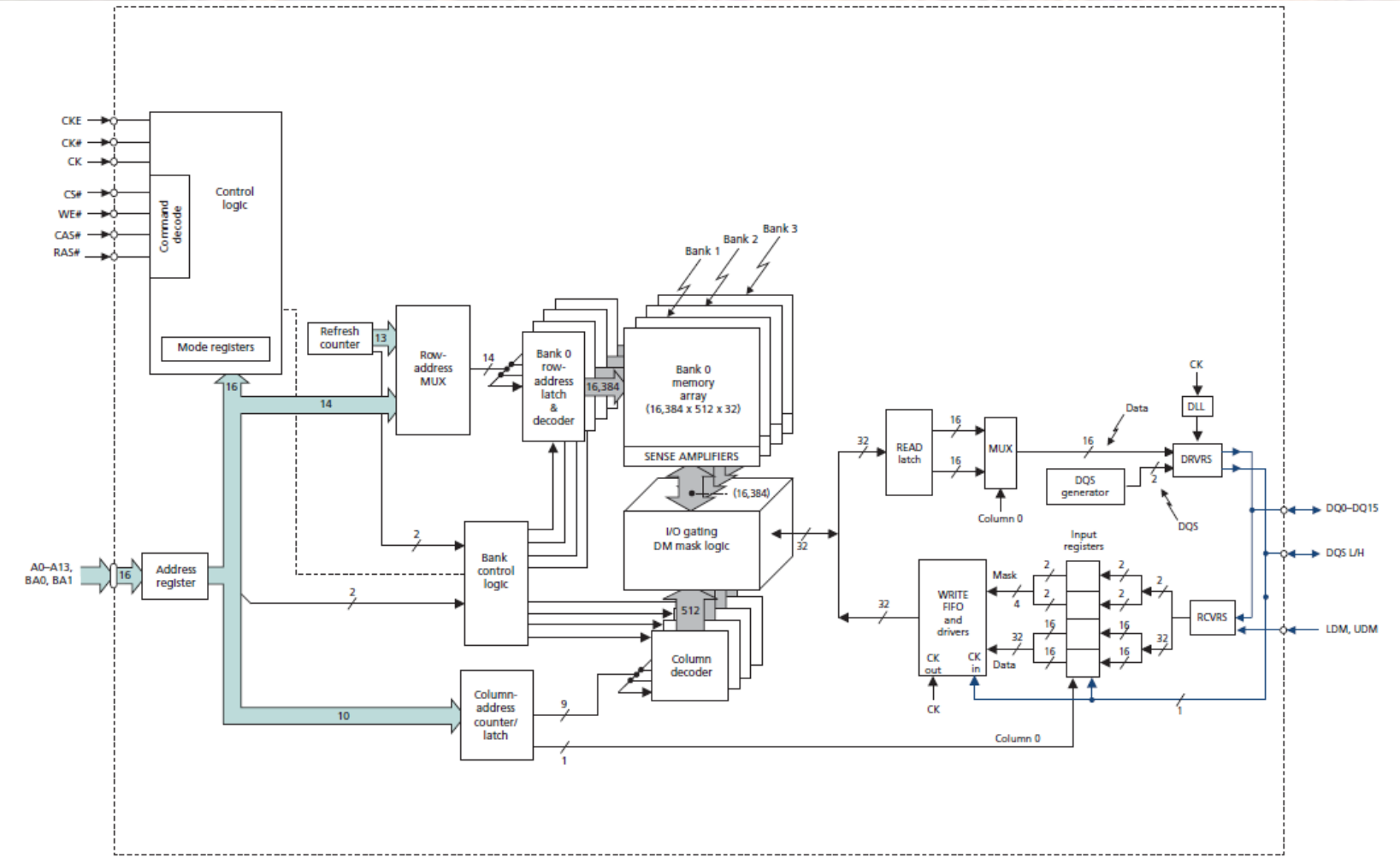
Memory - SDRAM

1Gb DDR SDRAM - 64M x 16



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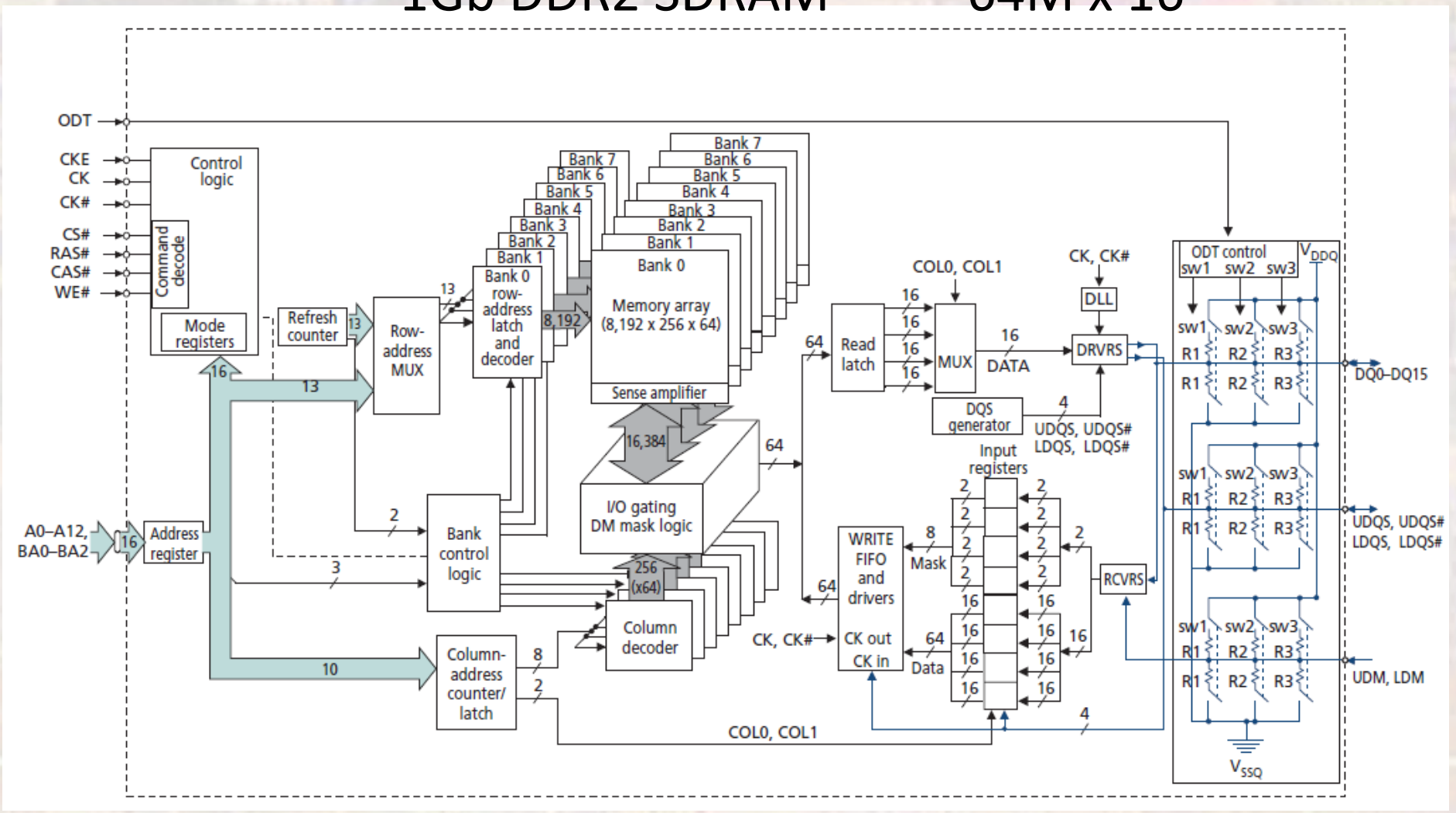
Memory - SDRAM

1Gb DDR2 SDRAM - 64M x 16



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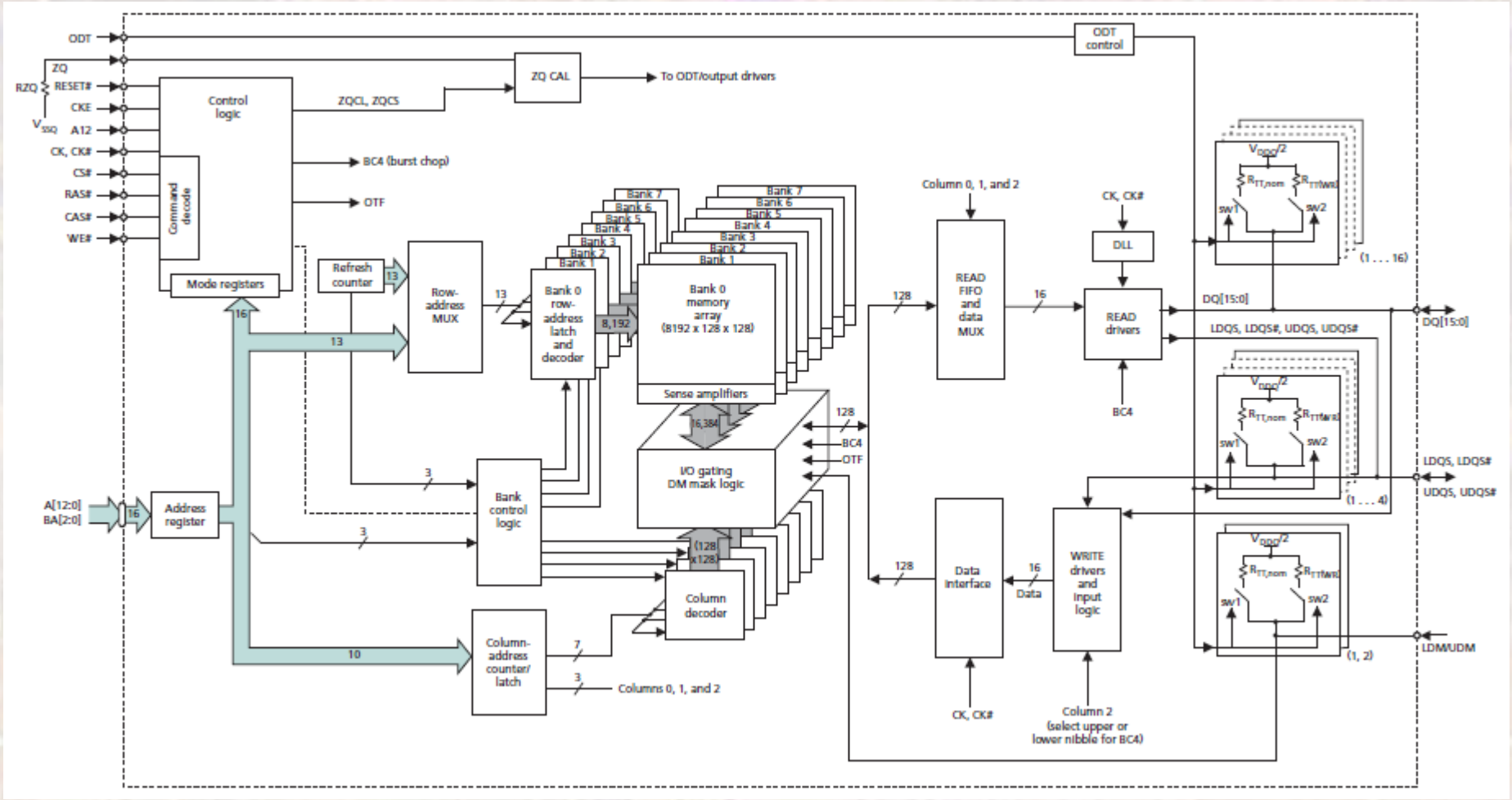
Memory - SDRAM

1Gb DDR3 SDRAM - 64M x 16



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