Memory - SRAM

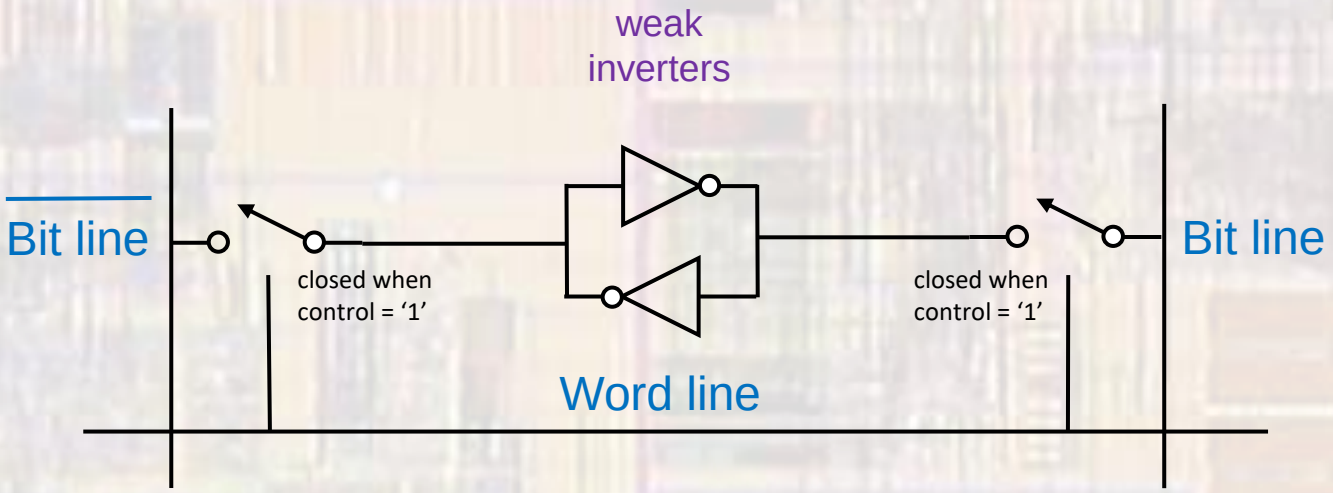
Last updated 4/14/21

Memory - SRAM

- Static Random Access Memory - SRAM
  - Key Attributes
    - Sequential vs. Random Access
    - Read only vs. Read/Write
    - Static vs. Dynamic
    - Volatile vs. non-Volatile
  - Key Measures
    - Density -
    - Speed +
    - Power -
    - Cost / bit -

Memory - SRAM

- SRAM – Circuit
  - Memory cell (1 bit) is based on a feedback circuit
  - Bit value is retained as long as power is maintained
  - Fastest read/write (R/W)
  - Highest power
  - Lowest density
  - Used in caches and small data memories



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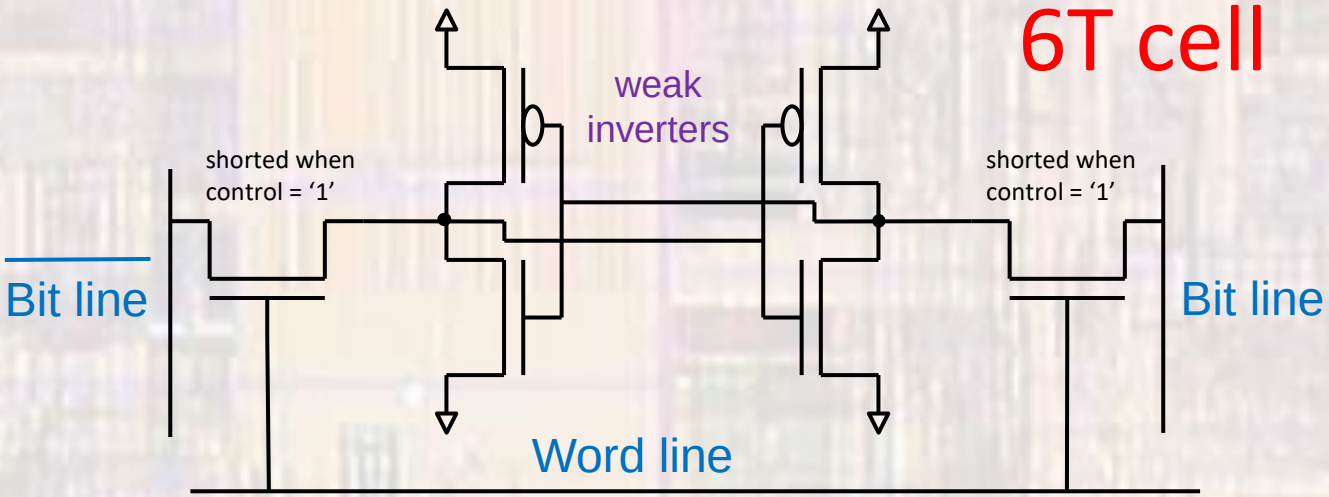
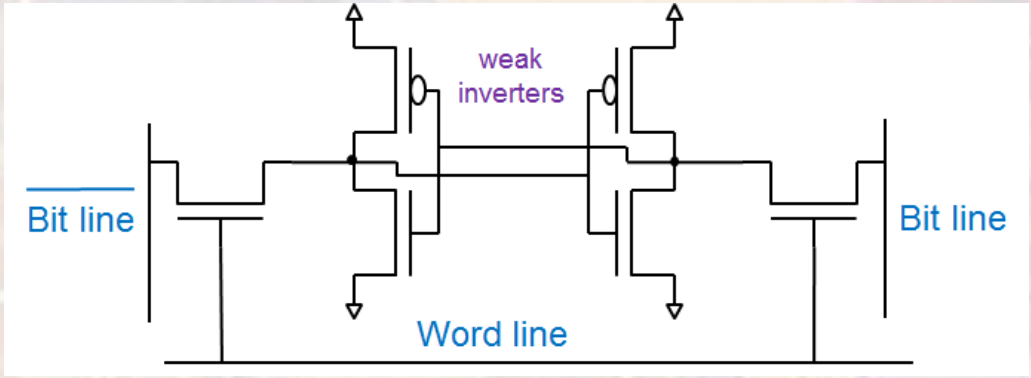
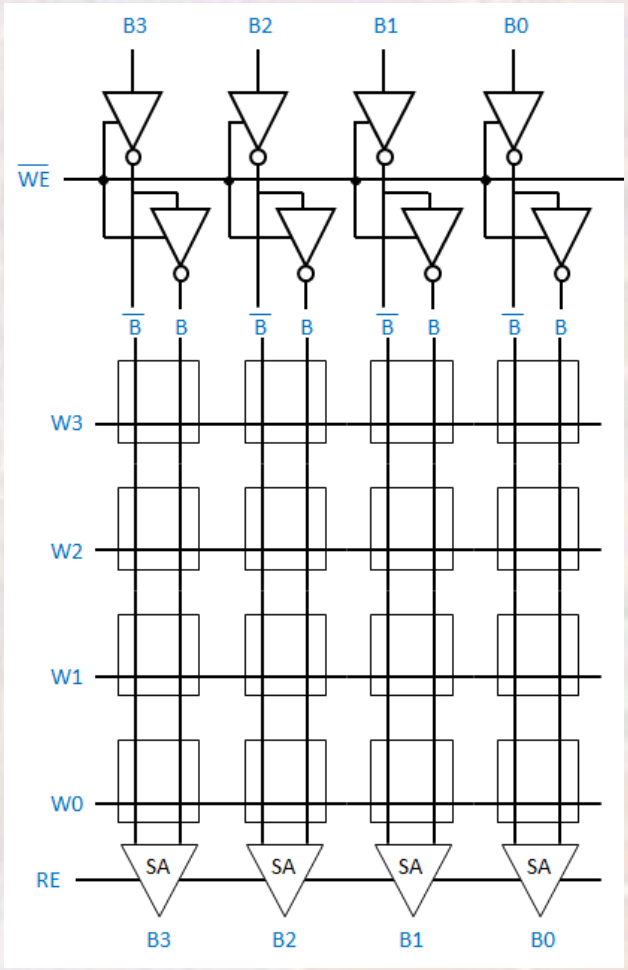


Memory - SRAM

- SRAM – Write
  - Read Enable (RE) disabled (low)
  - Place B0, B1, B2, B3 on inputs (data in)
  - Apply Address
    - Select the desired word line (high)
    - Select the desired column to input to
  - Strobe write enable bar ($\overline{WE}$) low
  - Bit lines override the bit cell inverters and store the new value in the cell



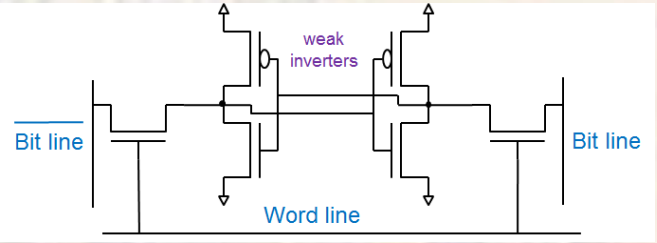


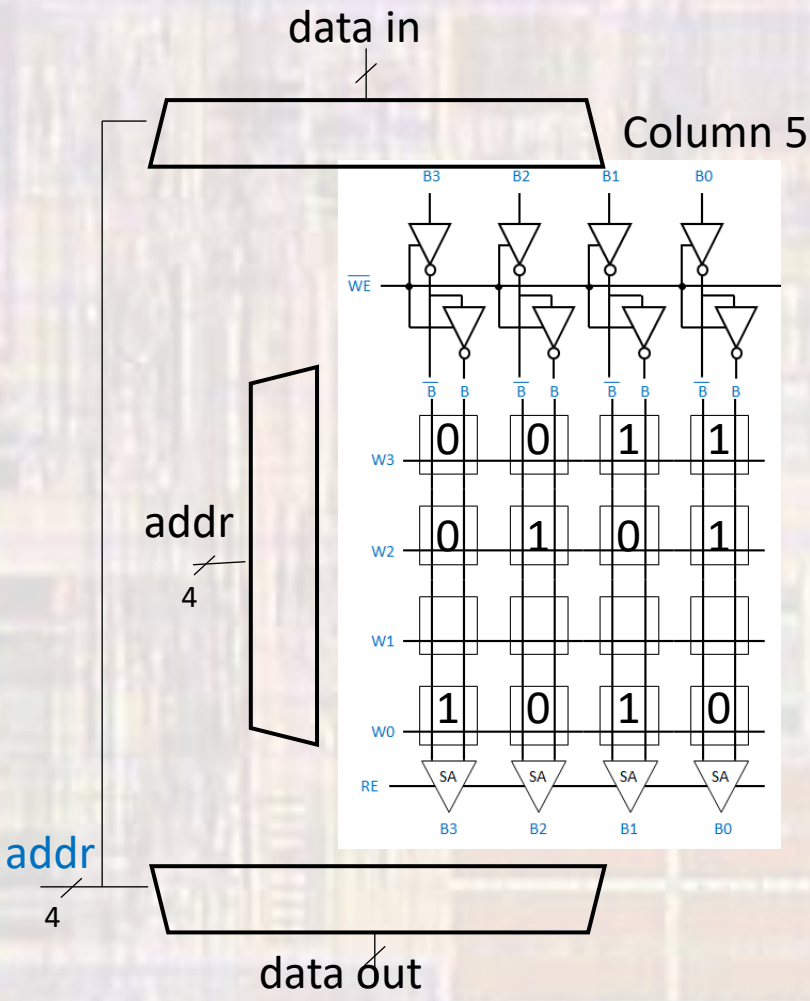
Memory - SRAM

- Write – x4 configuration – 16 x 16 x 4

R x C x b

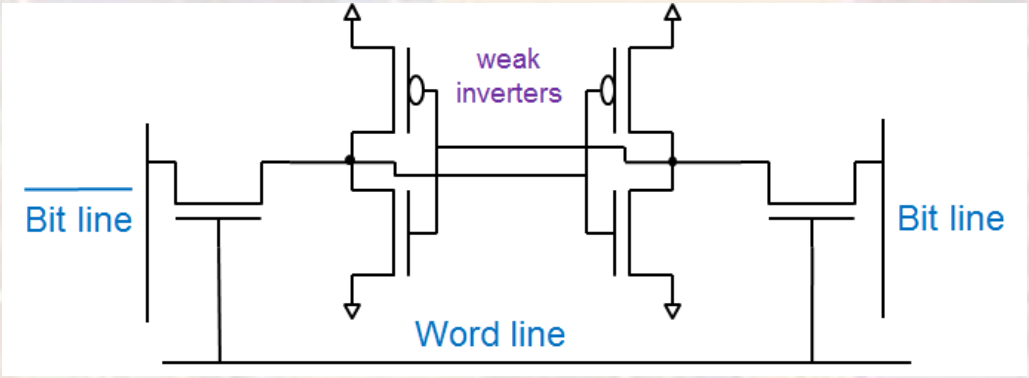
RE low data in = 0011 address = 35 00110101 WE – strobe	RE low data in = 0101 address = 25 00100101 WE – strobe	RE low data in = 1010 address = 5 00000101 WE – strobe

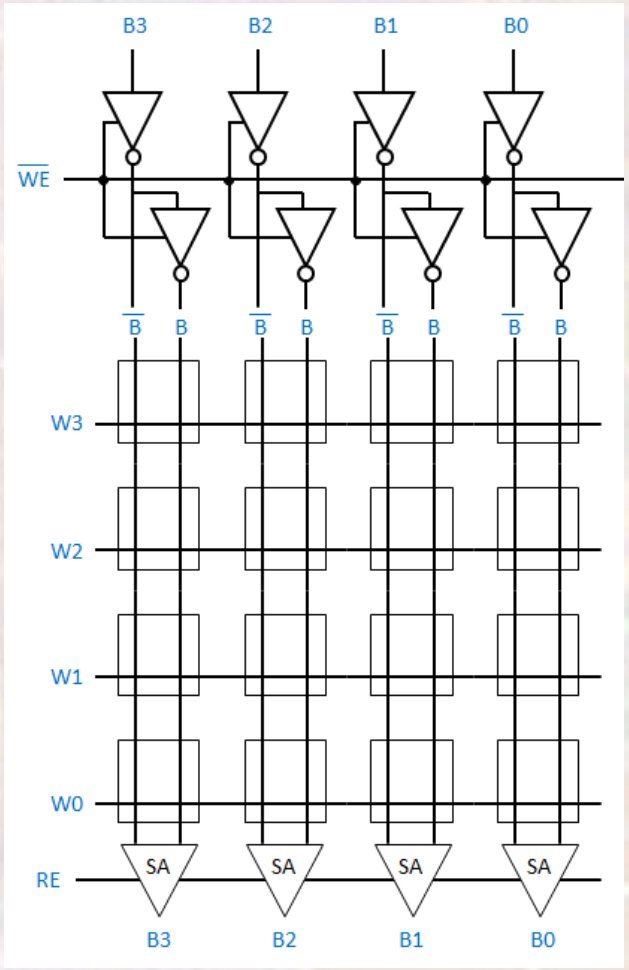




Memory - SRAM

- Read
  - Write enable bar ($\overline{WE}$) high
    - inverters tristated
  - Read Enable (RE) high
  - Apply Address
    - Select the desired word line (high)
    - Select the desired column to output
  - Bit cell inverters drive the bit lines and sense amplifiers read the value



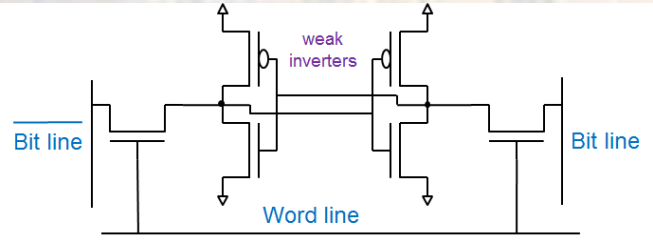


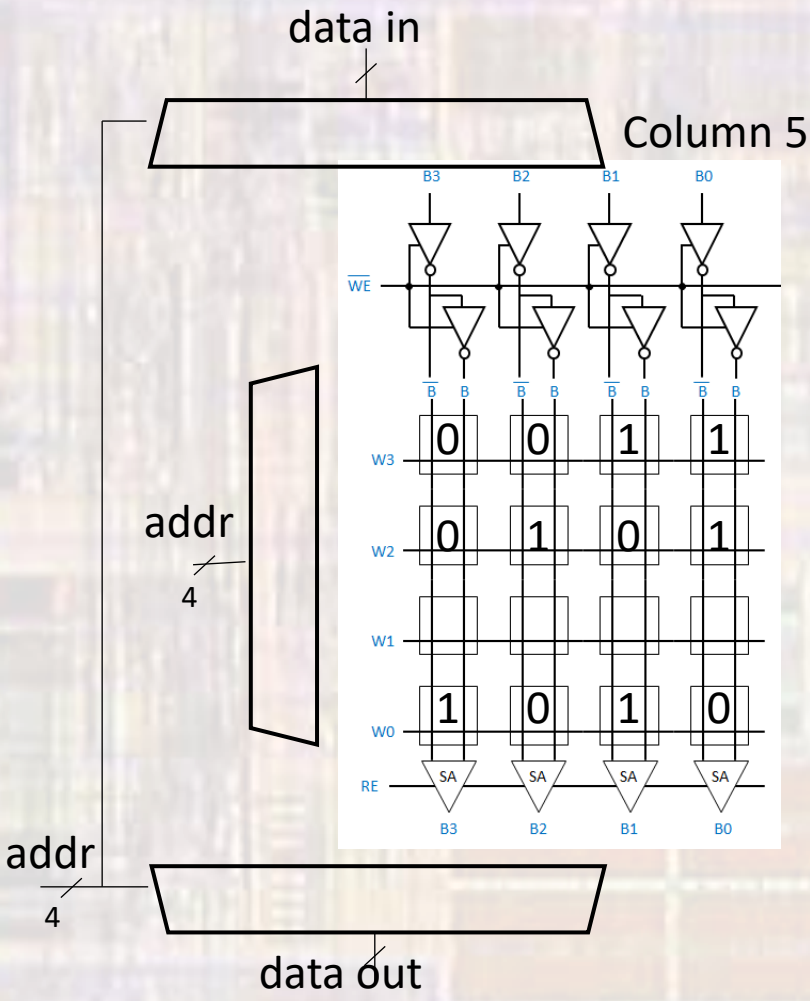
Memory - SRAM

- Read – x4 configuration – 16 x 16 x 4

R x C x b

WE' high RE high address = 35 00110101 → data out= 0011	WE' high RE high address = 25 00100101 → data out = 0101	WE' high RE high address = 5 00000101 → data out = 1010

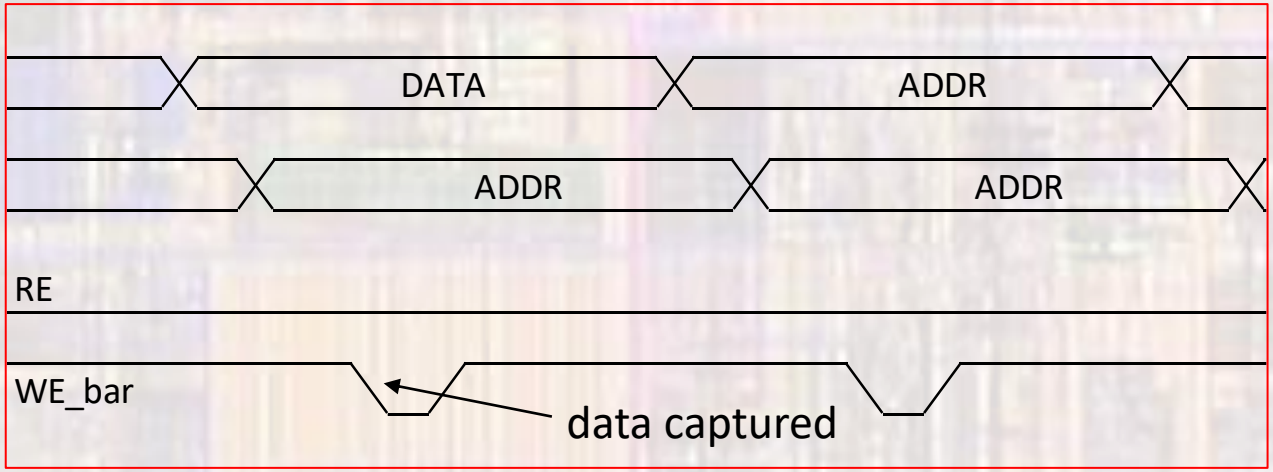




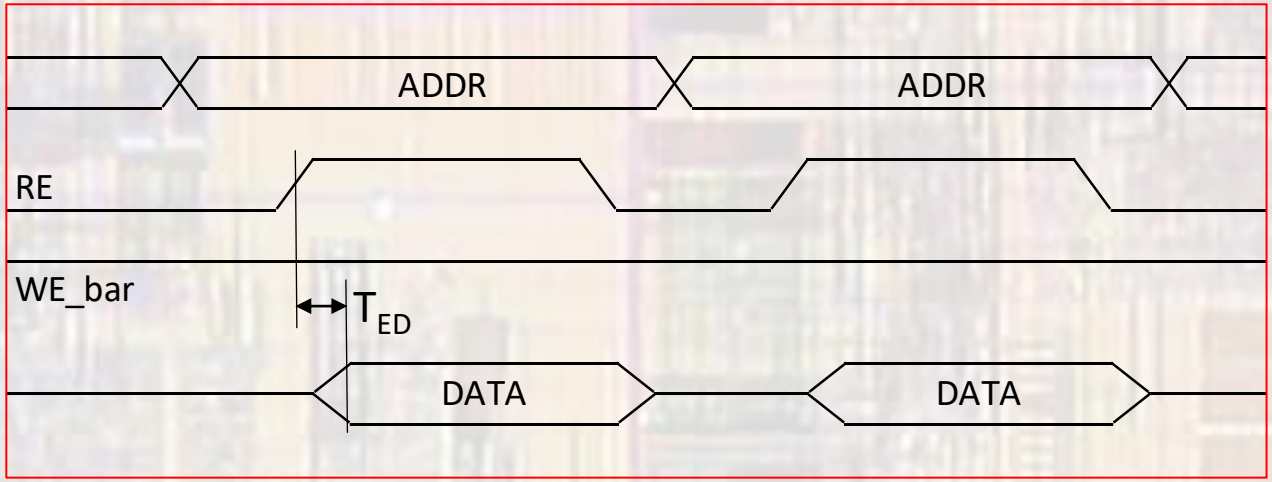
Memory - SRAM

- SRAM – Timing

WRITE

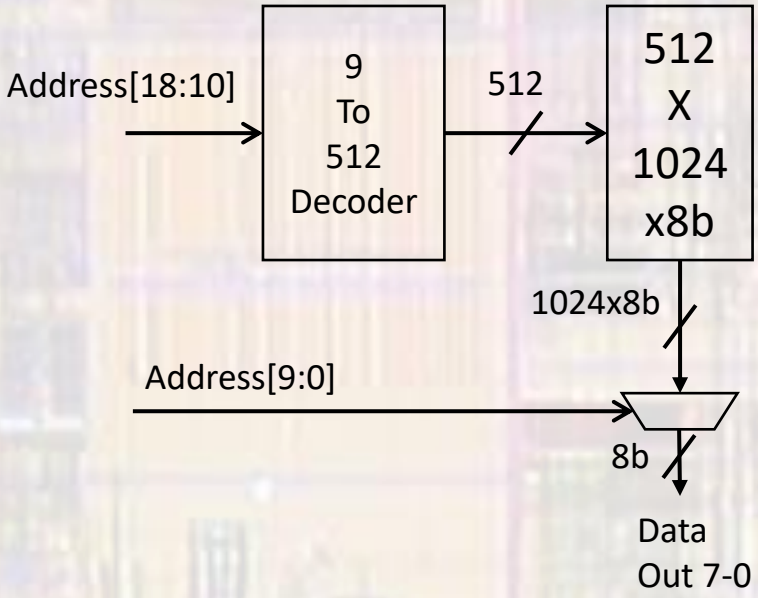


READ



Memory - SRAM

- SRAM – Complex configuration
  - Array Layout – 4Mb, in a x8 (4Mb, x8)
  - No address line sharing



Memory - SRAM

- SRAM – Complex configuration
  - Array Layout – 4Mb X 8 (4Mx8b) (implicit x1 format)
  - No address line sharing