

Single Cycle Processor Control

Last updated 4/14/21

Single Cycle Processor - Control

- ALU Control
- Basic ALU control mapping

Operation	invA	negB	ctl[1]	ctl[0]
AND	0	0	1	1
OR	0	0	1	0
NOR	1	1	1	1
NAND	1	1	1	0
ADD	0	0	0	1
SUB	0	1	0	1
SLT	0	1	0	0

Single Cycle Processor - Control

- ALU Control
- Full ALU control mapping

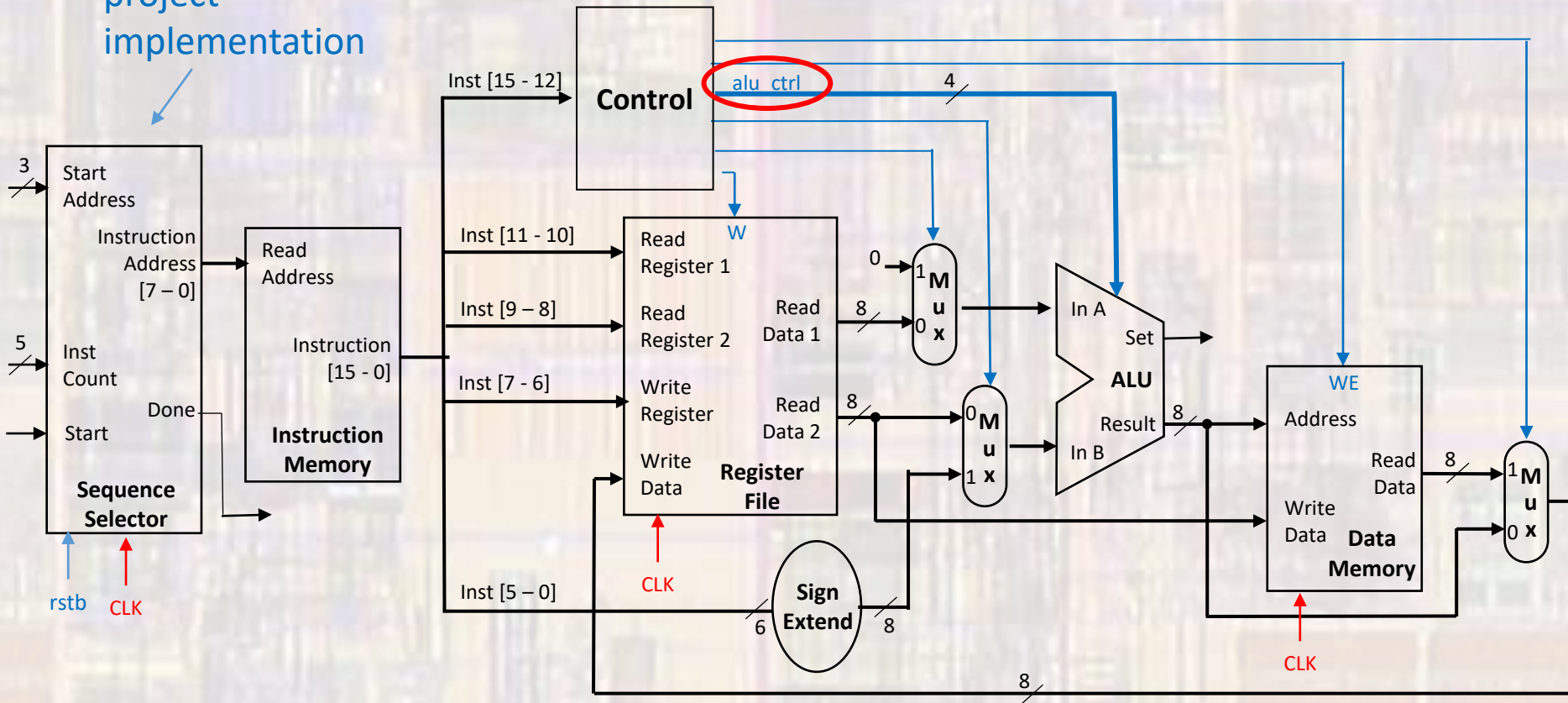
Operation	invA	negB	ctl[1]	ctl[0]
AND	0	0	1	1
OR	0	0	1	0
NOR	1	1	1	1
NAND	1	1	1	0
ADD	0	0	0	1
SUB	0	1	0	1
SLT	0	1	0	0
LD	0	0	0	1
ST	0	0	0	1
LDI	0	0	0	1

adding 0 from instruction
adding 0 from instruction
adding 0 from mux

Single Cycle Processor - Control

- ALU Control Signals

project implementation



Single Cycle Processor - Control

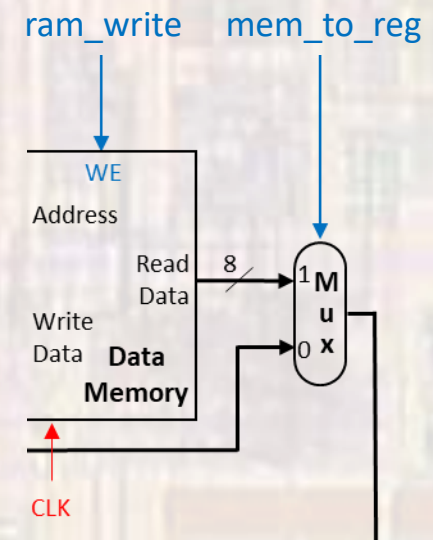
- Data Memory Control Signals

- mem_to_reg

- Selects between the ALU output and the RAM read data value to pass to the Write data input of the register file
- “1” only on LD instructions

- ram_write

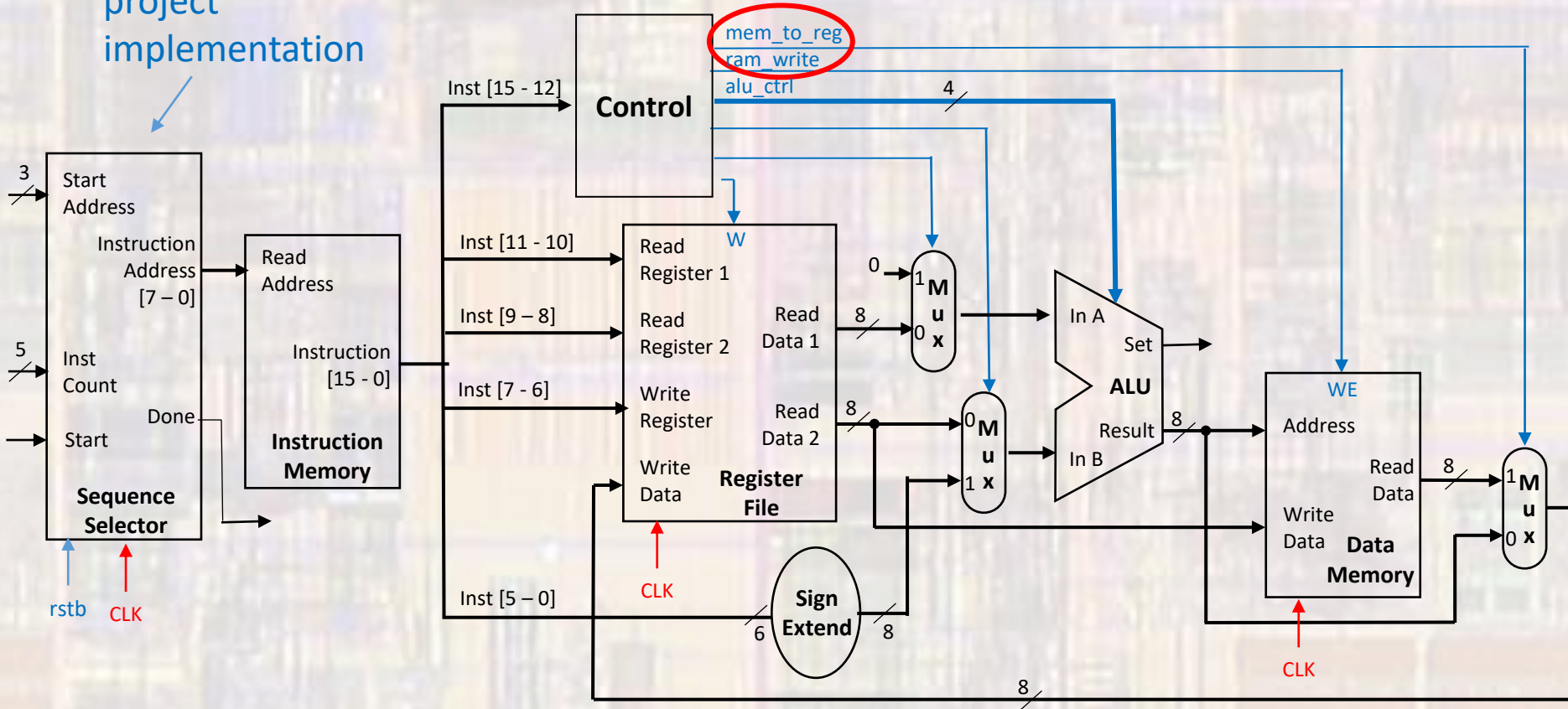
- Enable writing to the Data RAM
- “1” only on ST instructions



Single Cycle Processor - Control

- Data Memory Control Signals

project implementation



Single Cycle Processor - Control

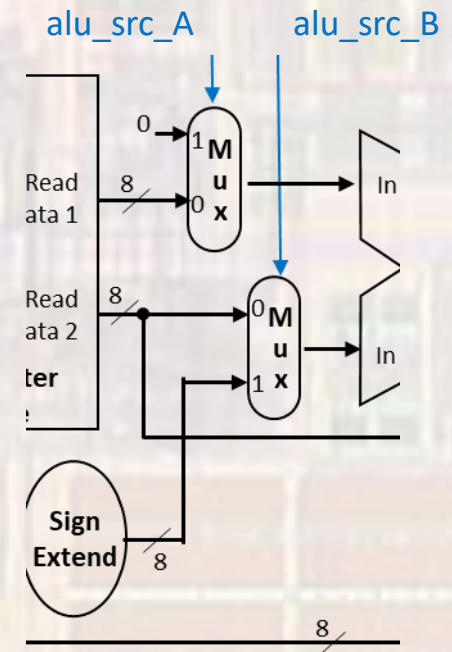
- ALU Input Control Signals

- alu_src_B

- Selects between the Read data 2 output of the register file and the sign extended immediate signal to pass to ALU input B
- “0” for arithmetic and logical instructions
- “1” for LD, ST and LDI instructions

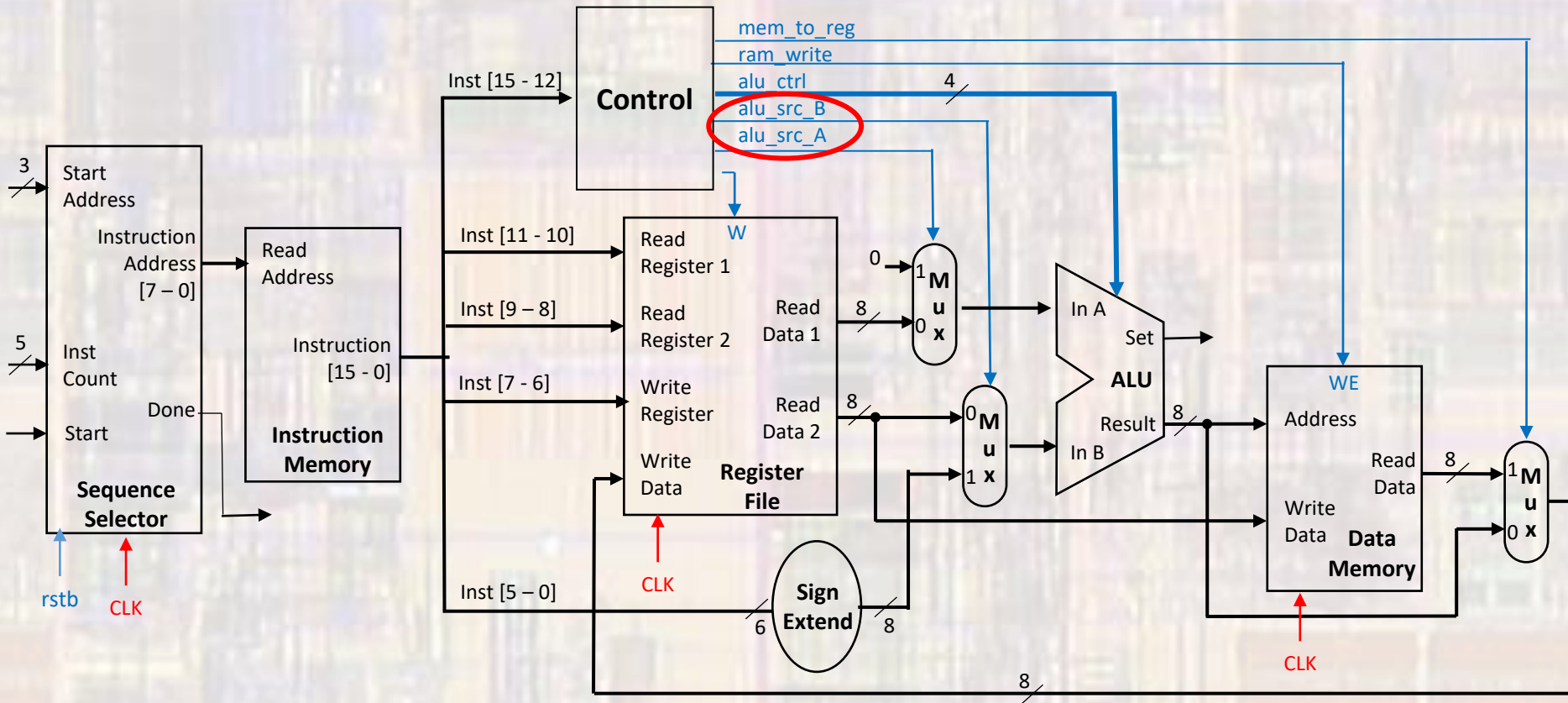
- alu_src_A

- Selects between the Read data 1 output of the register file and 0 to pass to ALU input A
- “1” only on LDI commands



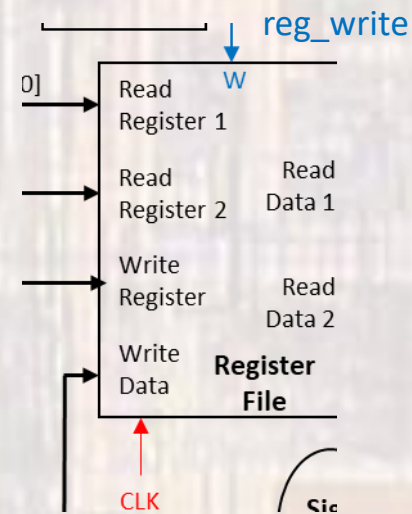
Single Cycle Processor - Control

- ALU Input Control Signals



Single Cycle Processor - Control

- Register File Control Signals
 - reg_write
 - Enable writing to the Register File
 - “0” only on ST and SLT instructions



Single Cycle Processor - Control

- Register File Control Signals

