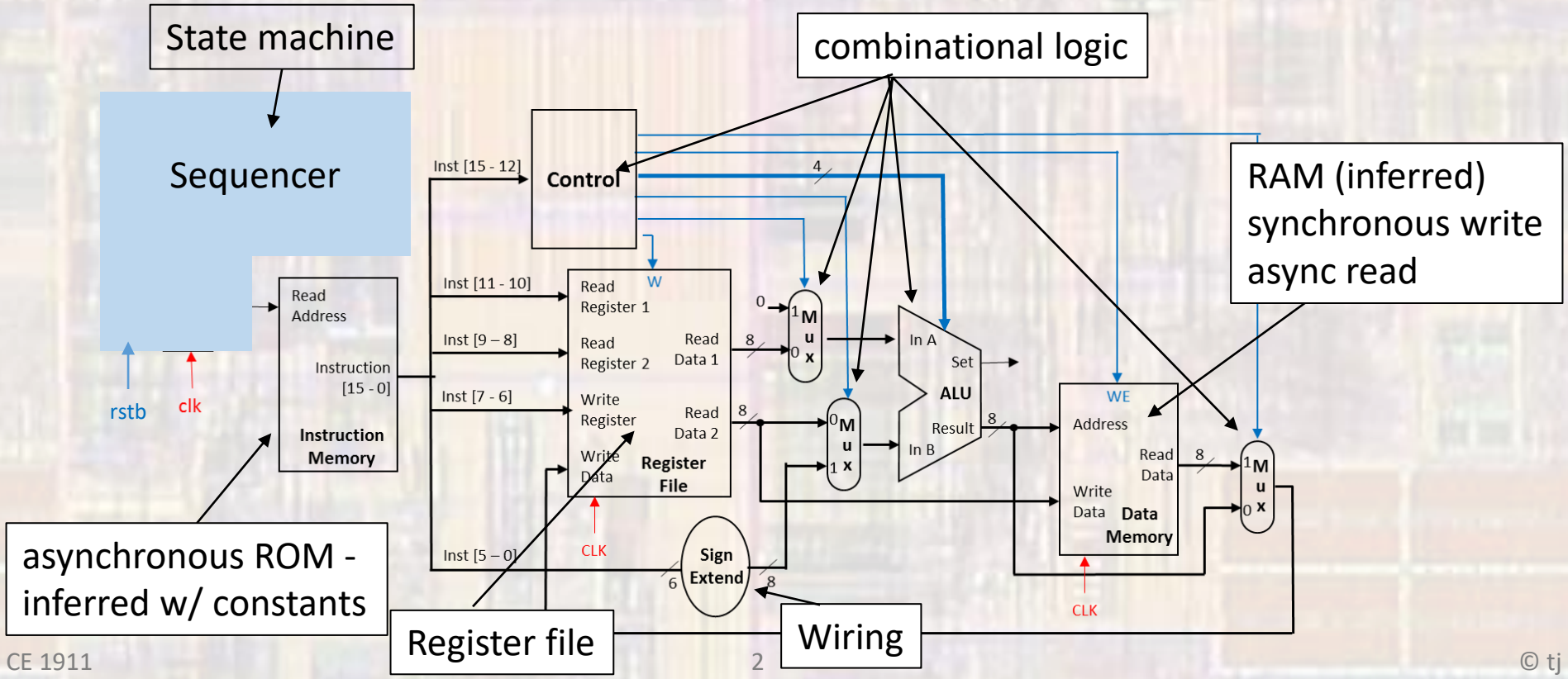
Single Cycle Processor Implementation

Last updated 4/22/21

Single Cycle Processor - Implementation

- Project
  - Build and test each block
    - except maybe the stand alone muxes and sign extend
  - Label all wires and use those names in the top level



Single Cycle Processor - Implementation

- Project
  - Register File
    - 4 additional outputs to directly pass RA, RB, RC, RD to SSEG
    - No rstb input
  - Sequencer
    - State machine – 3 states
    - reset – change switches – release reset
      - Starting address
      - Number of instructions to execute
    - start ↓(button) to start program
    - ONLY place rstb is used