State Machine Encoding HDL

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State Machine Encoding - HDL

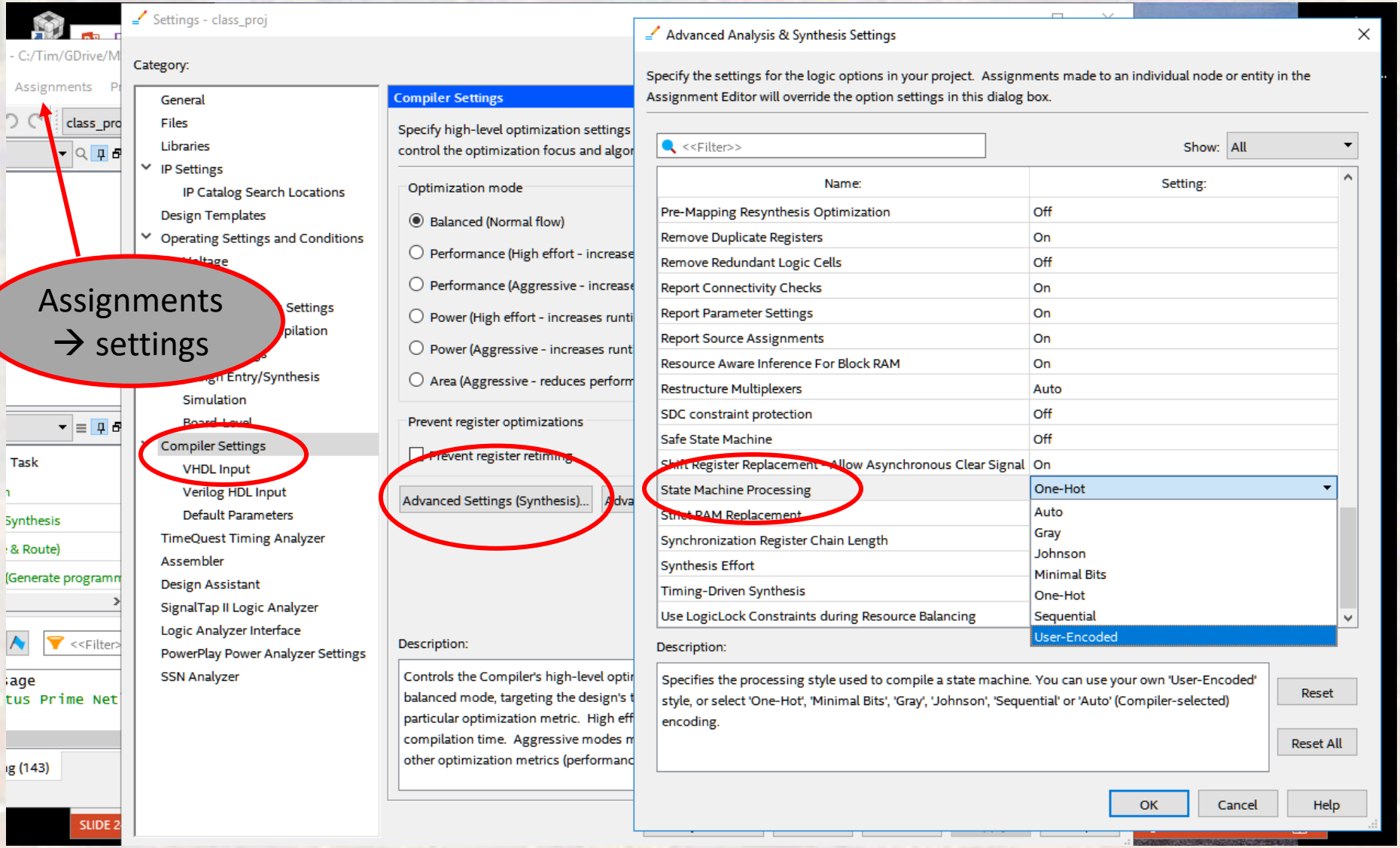
- Encoding
  - Comparison – considerations
    - Memory elements (bits) → area or fit
    - Coding / Decoding logic → area or fit
    - Speed
      - Shorter logic chains → faster maximum clock speeds
    - Power
      - P = v * i
      - P = v * c * dv/dt
      - dv/dt represents a transition 0 → 1
      - Fewer transitions → lower power

State Machine Encoding - HDL

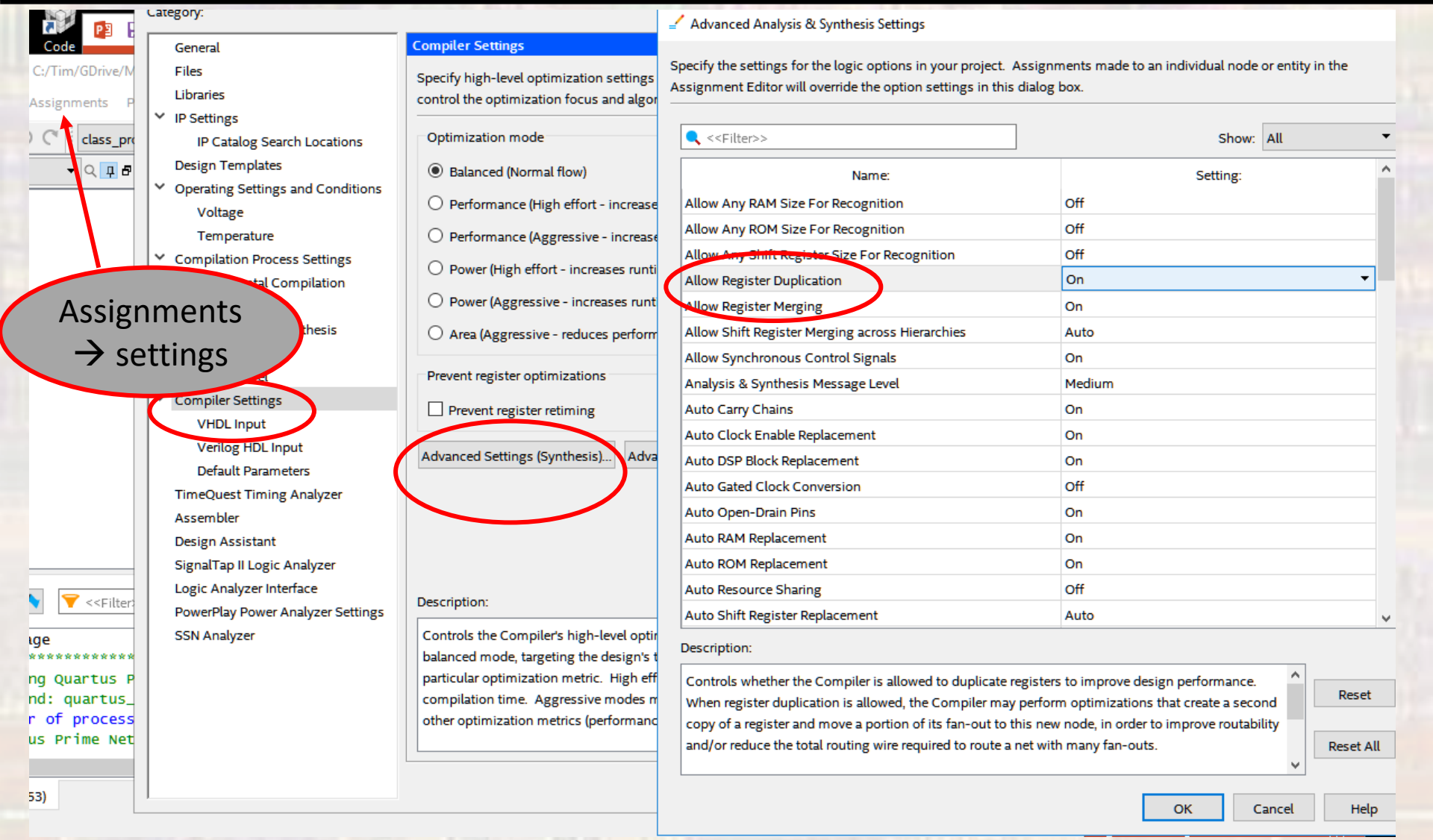
- Encoding – Quartus options

Auto	Allows the Compiler to choose the best encoding for the state machine.
Gray	Uses the minimal number of bits to encode the state machine, ceiling of 2 to the log of *n* states. This setting is difference from the **Minimal Bits** setting because each state has only one bit difference from its neighboring states.
Johnson	The number of bits used to encode the state machine is the ceilling of half of the states. Each state has only one bit difference from its neighboring states. Each state is generated by shifting the previous state's bits to the right by 1. The MSB of each state is the negation of the LSB of the previous state.
Minimal Bits	Uses the minimal number of bits to encode the state machine.
One-Hot	Encodes the state machine in the one-hot style. For one-hot encoding, the Quartus II software does not guarantee that each state has one bit set to one and all other bits to zero. Instead, the Quartus II software makes sure that the reset state is all-zeroes. All other states have two bits set to one and all others to zero. This is done so the state machine powers up in the reset state. This encoding has the same properties as true one-hot encoding: each state can be recognized by the value of one bit.
Sequential	Uses the minimal number of bits to encode the state machine; each state is the binary form of its state value.
User-Encoded	Encodes the state machine in the manner specified by the user.

State Machine Encoding - HDL



State Machine Encoding - HDL



State Machine Encoding - HDL

- Encoding
  - Comparison – Mod 10 counter

State Machine Encoding - HDL

- Encoding
  - Comparison – Mod 10 counter

    10 values (states) to encode

  - Binary (sequential)

    0000, 0001, 0010, 0011, 0100, 0101, 0110, 0111, 1000, 1001

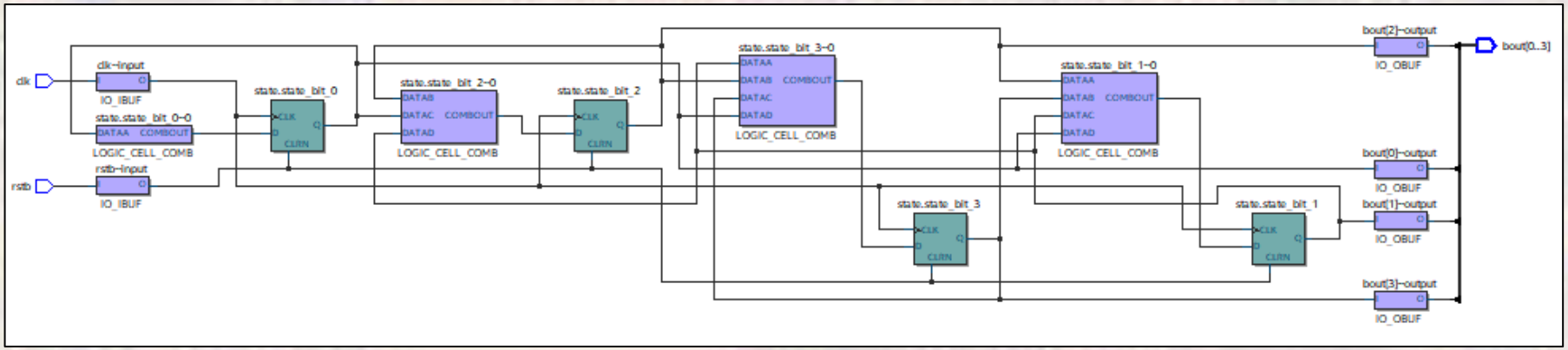
  - 4 registers
  - complex decoding
    - slower
    - bigger
  - multiple bit transitions

State Machine Encoding - HDL

- Encoding – Mod 10 counter

Binary

Total logic elements	5 / 49,760 (< 1 %)
Total registers	4



State Machine Encoding - HDL

- Encoding
  - Comparison – Mod 10 counter

    10 values to encode

  - One hot (cold)

    0000000000, 0000000011, 0000000101, 0000001001, 0000010001
    0000100001, 0001000001, 0010000001, 0100000001, 1000000001

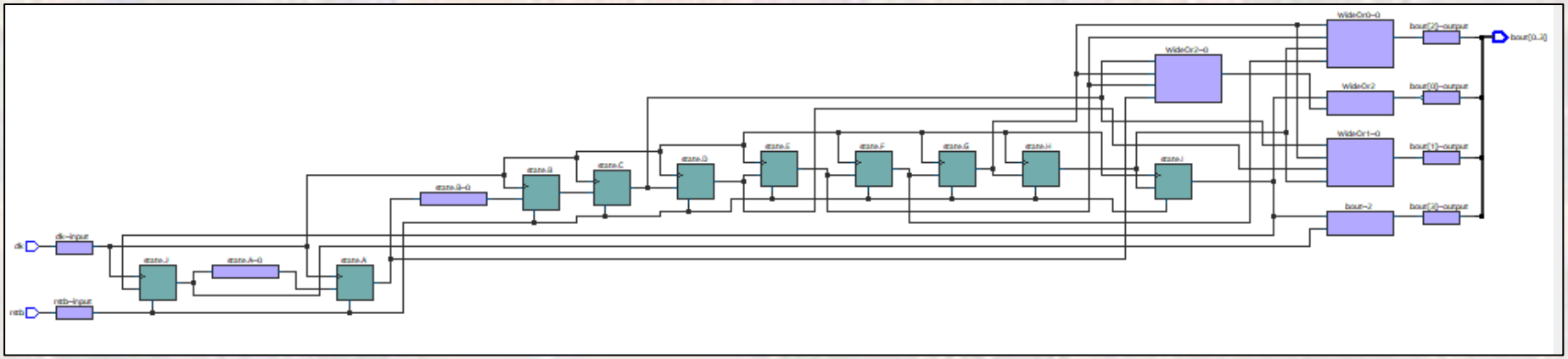
  - 10 registers
  - trivial decoding
    - faster
    - small
  - dual bit transitions

State Machine Encoding - HDL

- Encoding – Mod 10 counter

1-Hot

Total logic elements	12 / 49,760 (< 1 %)
Total registers	10



State Machine Encoding - HDL

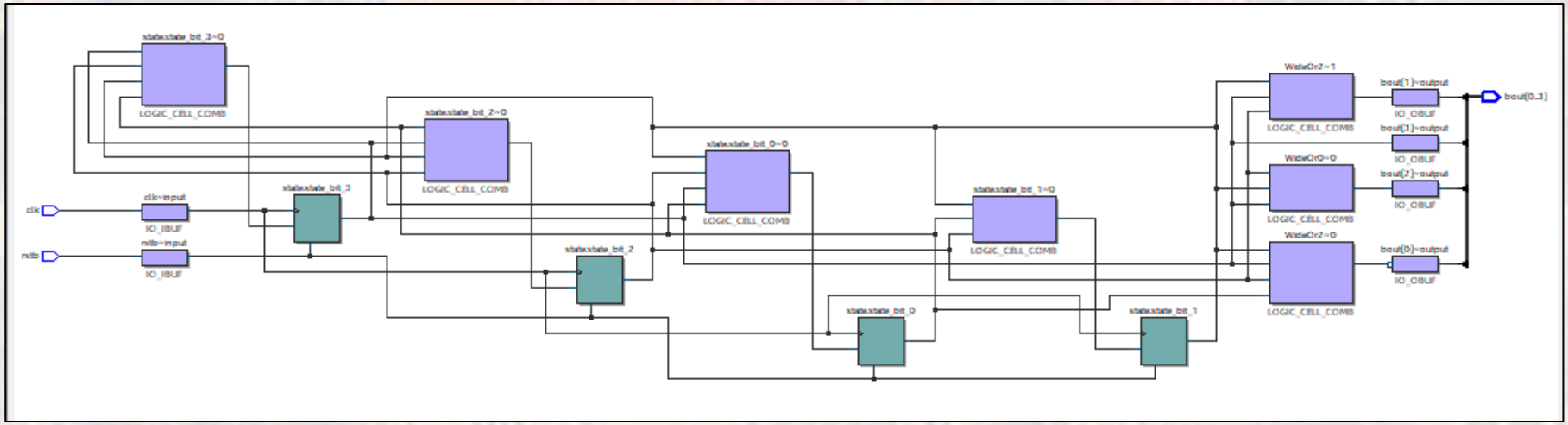
- Encoding
  - Comparison – Mod 10 counter
    10 values to encode
  - Gray
    0000, 0001, 0011, 0010, 0110, 0111, 0101, 0100, 1100, 1101
  - 4 registers
  - complex decoding
    - slower
    - larger
  - single bit transitions

State Machine Encoding - HDL

- Encoding – Mod 10 counter

Gray

Total logic elements	8 / 49,760 (< 1 %)
Total registers	4



State Machine Encoding - HDL

- Encoding
  - Comparison – Mod 10 counter

    10 values to encode

  - Johnson

    00000, 10000, 11000, 11100, 11110, 11111, 01111, 00111, 00011, 00001

  - 5 registers
  - complex decoding
    - slower
    - bigger
  - single bit transitions

State Machine Encoding - HDL

- Encoding – Mod 10 counter

Johnson

Total logic elements	15 / 49,760 (< 1 %)
Total registers	5