Last updated 1/28/21

- Manual Testbench
 - Results checked by hand
 - Simulation results in waveforms or output file
 - Check expected results to actual results by hand

- Automated Testbench
 - Results checked automatically
 - Code results into the test bench
 - Enumerated
 - Calculated
 - Check expected results to actual results in the testbench

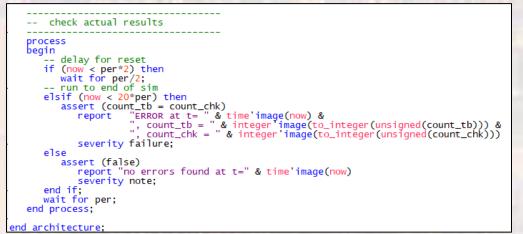
- Design Verification
 - Enumerated results
 - Explicitly list the expected results

```
counter_nbit_ud_tb1.vhdl
    by: johnsontimoj
    created: 6/28/2016
    version: 0.0
    test bench for 3 bit counter
    using enumerated results
     inputs: none
    outputs: count
    sim run time = 370 ns
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;
entity counter_nbit_ud_tb1 is
    generic(
               NN: integer := 3
    );
    -- no ports - tb
end entity;
architecture testbench of counter_nbit_ud_tb1 is
   signal clk_tb: std_logic;
signal dir_tb: std_logic;
signal dir_tb: std_logic := '0'; -- dir=0 is up
signal count_tb: std_logic_vector((NN-1) downto 0);
signal count_chk: std_logic_vector((NN-1) downto 0);
    constant per:
                          time := 20 ns;
    constant t_delay: time := 5 ns;
    constant t_reset: time := per*2;
```

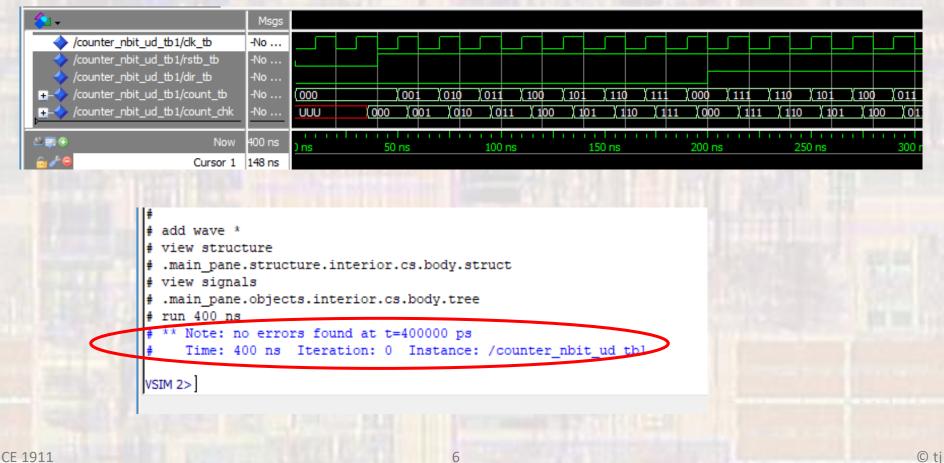
```
-- 3 bit counter prototype
  component counter_nbit_ud is
      generic(N: integer := 3);
      port ( i_clk:
                           in std_logic;
               i_rstb:
                           in std_logic;
                           in std_logic;
               i_dir:
                                              -- dir=0 is up
                           out std_logic_vector(N-1 downto 0)
               o_count:
           );
  end component;
begin
   -- Device Under Test
  dut: counter_nbit_ud
     generic map(
                  N => NN
     port map(
               i_clk => clk_tb,
               i_rstb => rstb_tb,
               i_dir => dir_tb,
               o_count => count_tb
     );
  -- Clock Process
  clk: process
     begin
         clk_tb <= '0';
         wait for PER/2;
         1000
            clk_tb <= not clk_tb;
           wait for per/2;
         end loop:
  end process;
  -- Reset process (active low)
  rstb: process
     begin
        rstb_tb <= '0';</pre>
        wait for t_reset;
        rstb_tb <= '1';
wait; -- only executes once
  end process;
  -- Direction process
  dir: process
     begin
        wait for t_reset;
        wait for per*8;
dir_tb <= not dir_tb;</pre>
      end process;
```

- Design Verification
 - Enumerated results
 - Explicitly list the expected results

generate expecte	ed results
"001 "010" "011" "100" "101" "111" "111" "100" "111" "101" "101" "101" "001" "001" "001" "001"	<pre>after t_reset-per/2 + per*0 + t_delay, after t_reset-per/2 + per*1 + t_delay, after t_reset-per/2 + per*2 + t_delay, after t_reset-per/2 + per*3 + t_delay, after t_reset-per/2 + per*5 + t_delay, after t_reset-per/2 + per*5 + t_delay, after t_reset-per/2 + per*6 + t_delay, after t_reset-per/2 + per*7 + t_delay, after t_reset-per/2 + per*8 + t_delay, after t_reset-per/2 + per*9 + t_delay, after t_reset-per/2 + per*10 + t_delay, after t_reset-per/2 + per*10 + t_delay, after t_reset-per/2 + per*11 + t_delay, after t_reset-per/2 + per*12 + t_delay, after t_reset-per/2 + per*13 + t_delay, after t_reset-per/2 + per*14 + t_delay, after t_reset-per/2 + per*15 + t_delay, after t_reset-per/2 + per*16 + t_delay, after t_reset-per/2 + per*16 + t_delay, after t_reset-per/2 + per*16 + t_delay, after t_reset-per/2 + per*17 + t_delay;</pre>



- Design Verification
 - Enumerated results



- Design Verification
 - Enumerated results
 - Changed expected result 4 from 3 to 7

<pre>//ounter_phit_ud_bi/ds_b //ounter_phit_ud</pre>	<mark>S</mark> +	Msgs												
<pre>//counter_rbst_ud_tbi/count_dbi</pre>		1												
<pre>c /counter_nbit_ud_bi/count_db / /counter_nbit_ud_bi/count_dk // / / / / / / / / / / / / / / / / / /</pre>	· · · · · · · · · · · · · · · · · · ·	1												
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- Design Verification
 - Calculated results

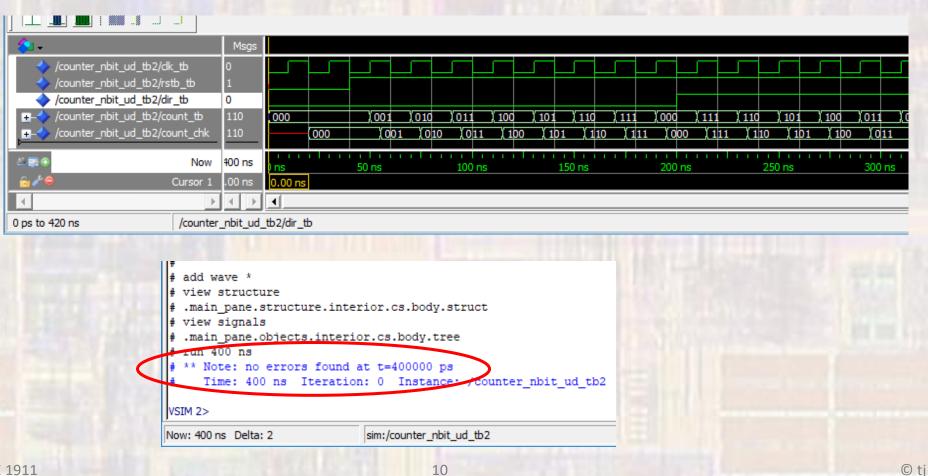
```
counter nbit ud tb2.vhd]
     by: johnsontimoj
     created: 6/28/2016
    version: 0.0
    test bench for 3 bit counter
    using calculated results
     inputs: none
    outputs: count
    sim run time = 370 ns
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;
entity counter_nbit_ud_tb2 is
    generic(
               NN: integer := 3
    ):
    -- no ports - tb
end entity;
architecture testbench of counter_nbit_ud_tb2 is
   signal clk_tb: std_logic;
signal rstb_tb: std_logic;
signal dir_tb: std_logic := '0'; -- dir=0 is up
signal count_tb: std_logic_vector((NN-1) downto 0);
signal count_chk: std_logic_vector((NN-1) downto 0);
    constant per:
                        time := 20 ns;
    constant t_delay: time := 5 ns;
    constant t_reset: time := per*2;
```

```
-- 3 bit counter prototype
   component counter_nbit_ud is
      generic(N: integer := 3);
      port ( i_clk:
                             in std_logic;
                i_rstb:
                             in std_logic;
                             in std_logic; -- dir=0 is up
out std_logic_vector(N-1 downto 0)
                i_dir:
                o_count:
             ):
   end component;
begin
   -- Device Under Test
   _____
   dut: counter_nbit_ud
      generic map(
                   N => NN
     port map(
    i_clk => clk_tb,
    i_rstb => rstb_tb,
    -> dir_tb,
                o_count => count_tb
      );
   -- Clock Process
   clk: process
      begin
         clk_tb <= '0';
         wait for PER/2;
          1000
             clk_tb <= not clk_tb;
             wait for per/2;
         end loop;
   end process;
   -- Reset process (active low)
   rstb: process
      begʻin
         rstb_tb <= '0';</pre>
         wait for t_reset;
         rstb_tb <= '1';
wait: -- only executes once
   end process:
   -- Direction process
   dir: process
      begin
         wait for t_reset;
         wait for per*8;
         dir_tb <= not dir_tb;
      end process;
```

- Design Verification
 - Calculated results

```
generate expected results
   process
   begin
       if (rstb_tb = '0') then
  count_chk <= (others => '0');
       wait for per*3/4;
else if (dir_tb = '0') then
               count_chk <= std_logic_vector(unsigned(count_chk) + 1);</pre>
           else
               count_chk <= std_logic_vector(unsigned(count_chk) - 1);</pre>
           end if;
       end if:
       wait for per;
   end process;
    -- check actual results
   process
   begin
       -- delay for reset
       if (now < per*2.5) then
  wait for per/2;</pre>
       -- run to end of sim
       elsif (now < 20*per) then
           assert (count_tb = count_chk)
                          "ERROR at t= " & time'image(now) &
", count_tb = " & integer'image(to_integer(unsigned(count_tb))) &
", count_chk = " & integer'image(to_integer(unsigned(count_chk)))
               report
               severity failure;
       else
           assert (false)
               report "no errors found at t=" & time'image(now)
               severity note;
       end if:
       wait for per;
   end process;
end architecture;
```

- Design Verification
 - Calculated results



10