C-MOS Circuit Parametrics

Last updated 4/12/22

C-MOS Circuits

- Parameters $K_n = \frac{W\mu_n C_{ox}}{2L}$ $\qquad$ $K_p = \frac{W\mu_p C_{ox}}{2L}$

$$K_n = \frac{k'_n}{2}\frac{W}{L} \qquad k'_n = \mu_n C_{ox} \qquad K_p = \frac{k'_p}{2}\frac{W}{L} \qquad k'_p = \mu_p C_{ox}$$

$\mu_n,\ \mu_p, C_{ox}$ fixed for a given semiconductor process →

k'_n , k'_p fixed for a given semiconductor process

$$I_D = K_n[2(V_{GS} - V_{tn})V_{DS} - V_{DS}^2] \qquad I_D = K_p[2(V_{SG} - V_{tp})V_{SD} - V_{SD}^2]$$

$$I_D = \frac{k'_n}{2}\frac{W}{L}[2(V_{GS} - V_{tn})V_{DS} - V_{DS}^2] \qquad I_D = \frac{k'_p}{2}\frac{W}{L}[2(V_{SG} - V_{tp})V_{SD} - V_{SD}^2]$$

$V_{DSsat} = V_{GS} - V_{th}$ $\qquad$ $V_{SDsat} = V_{SD} - V_{th}$

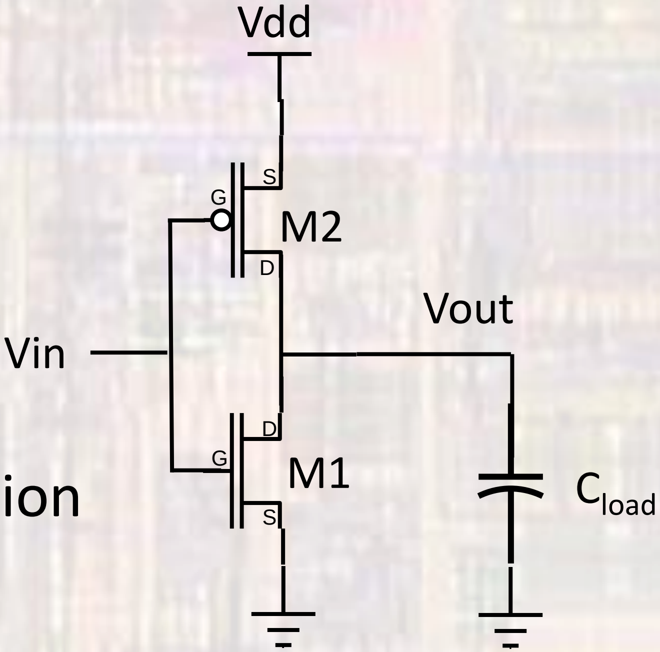
$$I_D = K_n(V_{GS} - V_{tn})^2 \qquad I_D = K_p(V_{SG} - V_{tp})^2$$

$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_{tn})^2 \qquad I_D = \frac{k'_p}{2}\frac{W}{L}(V_{SG} - V_{tp})^2$$

$$C_{Gn} = W \times L \times {}^{k'_n}/_{\mu_n} \qquad C_{Gp} = W \times L \times {}^{k'_p}/_{\mu_p}$$

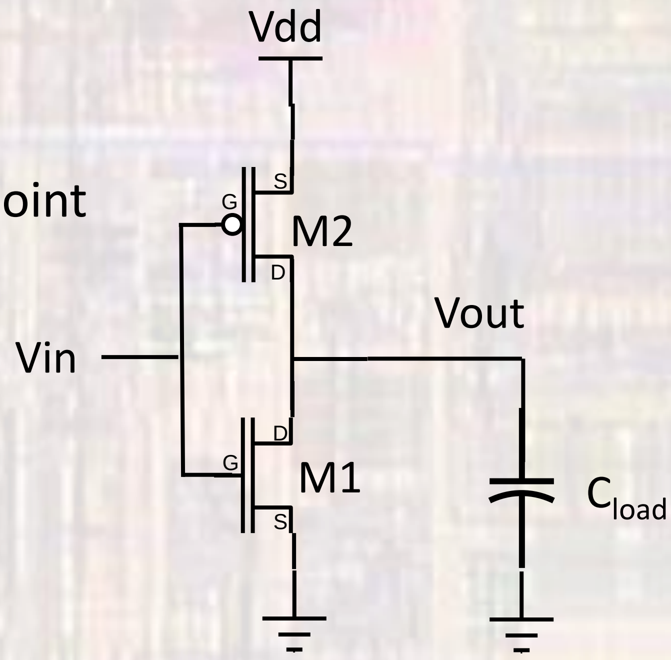
C-MOS Circuits

- Switching speeds
  - Midpoint in to midpoint out
    - tphl, tplh
  - Assume only one device active
    - Charging/discharging the capacitor
  - Devices start in saturation and transition to non-saturation



C-MOS Circuits

- Switching speeds
  - Super simple estimation
    - Assume in saturation upto the switching point



$$I = C\frac{dv}{dt} = \frac{k'_n}{2}\frac{W}{L}(V_{gs} - V_t)^2$$

$$I = C\frac{dv}{dt} = \frac{k'_n}{2}\frac{W}{L}(V_{dd} - V_t)^2$$

$$dt = C\frac{1}{\frac{k'_n}{2}\frac{W}{L}(V_{dd} - V_t)^2}dv$$

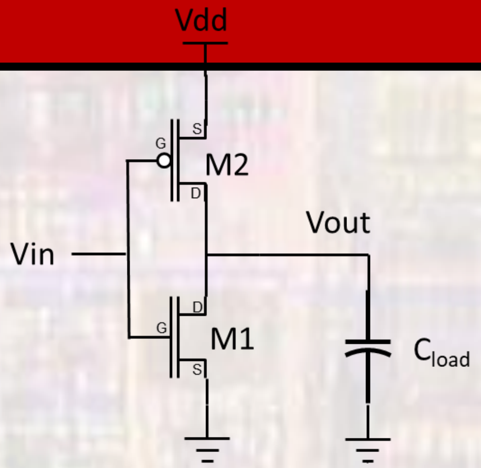
$$t_{hl} = C\frac{1}{\frac{k'_n}{2}\frac{W}{L}(V_{dd} - V_t)^2}\frac{Vdd}{2}$$

$$t_{lh} = C\frac{1}{\frac{k'_p}{2}\frac{W}{L}(V_{dd} - V_t)^2}\frac{Vdd}{2}$$

$$t_{pd} = t_{hl} + t_{lh}$$

C-MOS Circuits

- Switching speeds
  - Super simple estimation
    - Assume in saturation upto the switching point



$$t_{hl} = C\frac{1}{\frac{k'_n}{2}\frac{W}{L}(V_{dd}-V_t)^2}\frac{Vdd}{2}$$

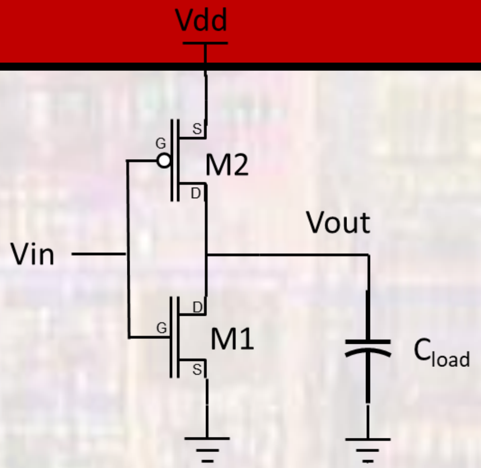
$$t_{lh} = C\frac{1}{\frac{k'_p}{2}\frac{W}{L}(V_{dd}-V_t)^2}\frac{Vdd}{2}$$

$$t_{pd} = t_{hl} + t_{lh}$$

- Assuming N and P matched for switching point

$$t_{pd} = \frac{C\,V_{dd}}{\frac{k'_n}{2}\frac{W}{L}(V_{dd}-V_t)^2}$$

C-MOS Circuits



- Switching speeds
  - Super simple estimation
    - Assume in saturation upto the switching point
    - Matched devices

$$t_{pd} = \frac{C_{load}\,V_{dd}}{\frac{k'_n}{2}\frac{W}{L}(V_{dd}-V_t)^2}$$

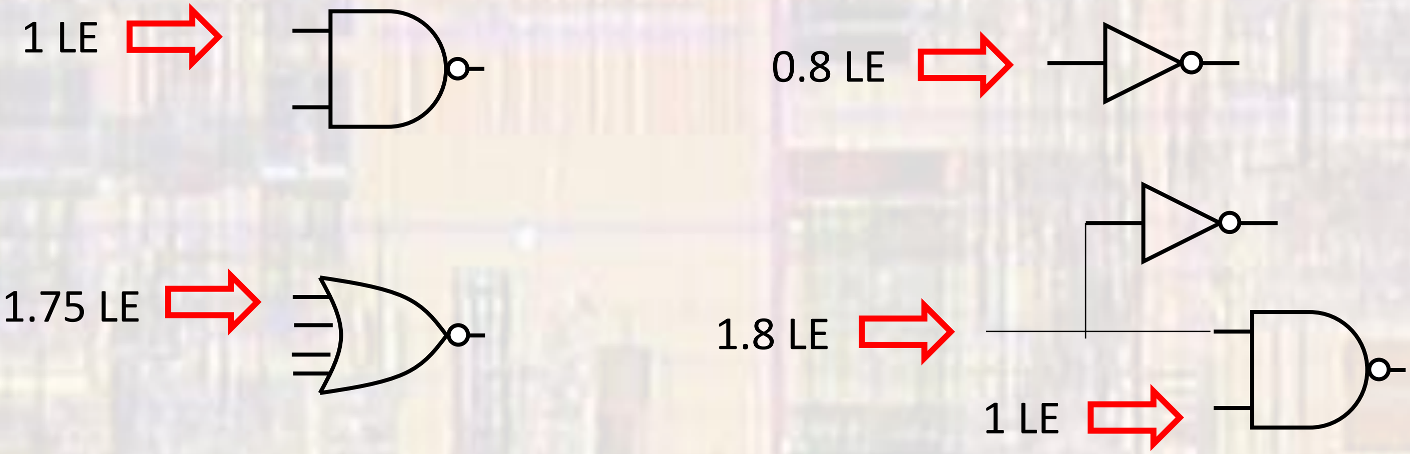
    - Reduce tpd
      - Increase V_{dd}
      - Increase W/L
      - Decrease C_{load}

Increasing Vdd reduces gate delays
→ higher operating frequency

Logic Timing

- Gate level timing

  - Each gate **input** has an equivalent input load factor
    - Models the input capacitance
    - Load equivalent (LE)
    - Technology / Process dependent


1 LE

0.8 LE

1.75 LE

1.8 LE

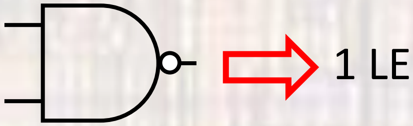
1 LE

Logic Timing

- Gate level timing

  - Each gate has internal delay
    - Assumes a fixed external load – 1 LE
    - Circuit dependent – but fixed
    - Technology / Process dependent

$t_{pd_{inv}}$

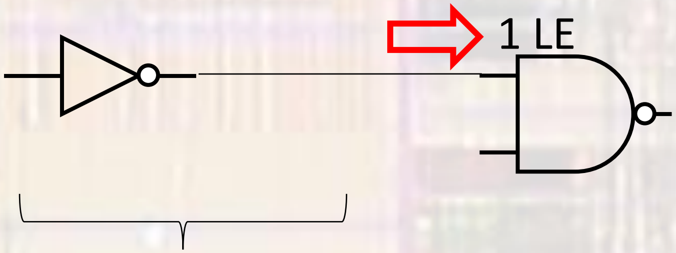


$t_{pd_{nand}}$

Logic Timing

- Gate level timing

  - Each gate has a variable delay factor - r
    - Function of the gate’s drive capability
    - Modifies the circuit delay based on the amount of loading
    - Circuit dependent

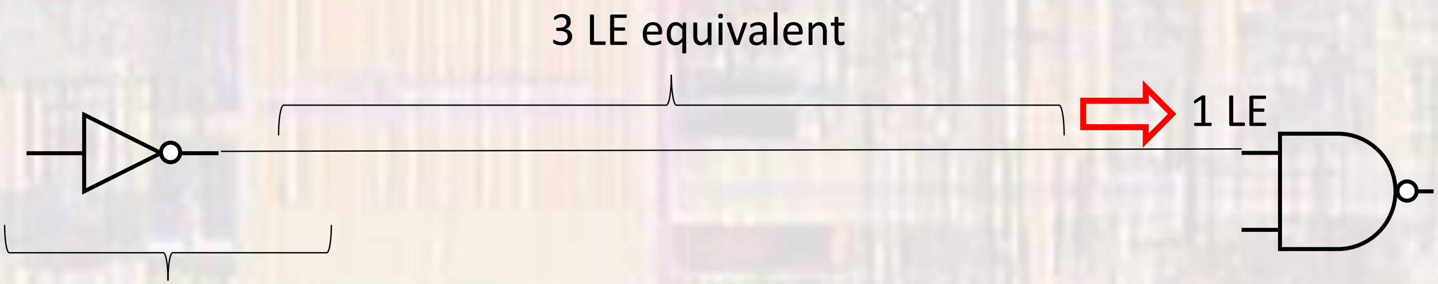


$$\underbrace{t_{pd_{inv}}}_{} + r \times 1\ \mathrm{LE}$$

Logic Timing

- Gate level timing

  - Long wires have enough capacitance to impact delays
    - Model long wires in terms of load equivalents (LEs)
    - Modifies the circuit delay based on the amount of loading
    - Circuit dependent



$$t_{pd_{inv}} + r \times (3\ \mathrm{LE} + 1\ \mathrm{LE})$$

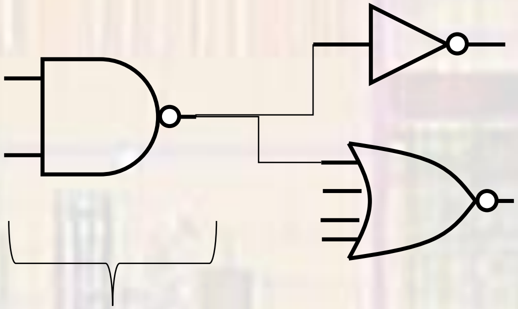
Digital Circuit Timing

- Gate level timing

$$t_{pd} = t_{fixed\_delay} + r_{variable\_delay\_factor} * \text{ Load Equivalents}$$

Standard

Gate	INV	2-NAND	2-NOR	4-NAND	4-NOR
Input load factor (LE)	0.8	1.0	2.0	1.66	3.33
Fixed delay factor	50ps	65ps	65ps	80ps	80ps
Variable delay factor	5ps/LE	8ps/LE	8ps/LE	12ps/LE	12ps/LE



$$t_{pd} = 65ps + 8ps/LE*(0.8LE + 3.33LE) = 98ps^{**}$$

** we are assuming interconnect capacitance is negligible

Digital Circuit Timing

- Gate level timing

$$t_{pd} = t_{fixed\_delay} + r_{variable\_delay\_factor} * \text{Load Equivalents}$$

Standard

Gate	**INV**	**2-NAND**	**2-NOR**	**4-NAND**	**4-NOR**
Input load factor (LE)	0.8	1.0	2.0	1.66	3.33
Fixed delay factor	50ps	65ps	65ps	80ps	80ps
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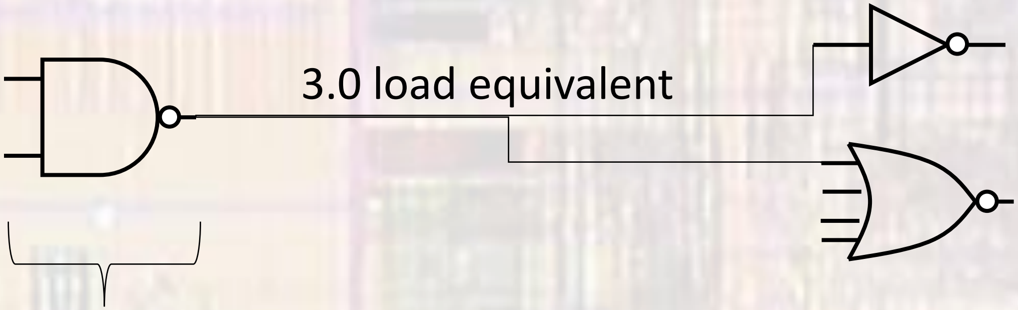
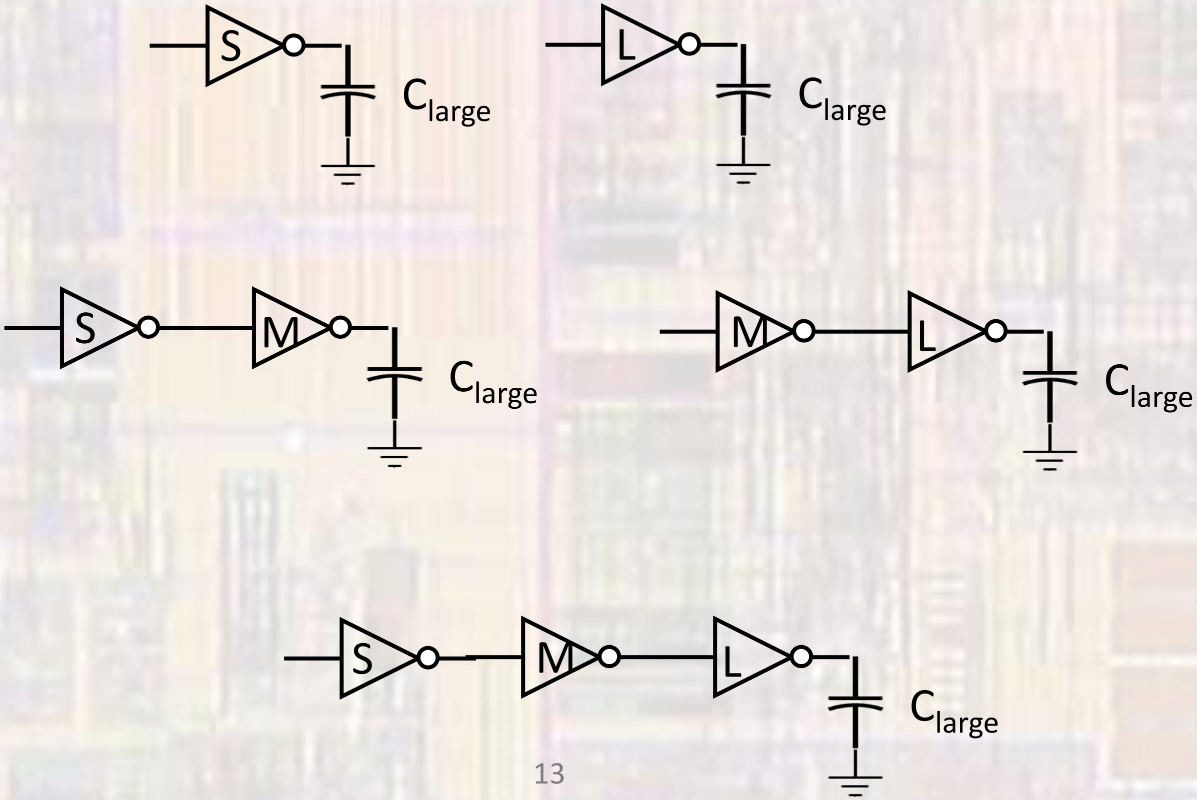


$$t_{pd} = 65ps + 8ps/LE*(0.8LE + 3.33LE + 3.0LE) = 122ps$$

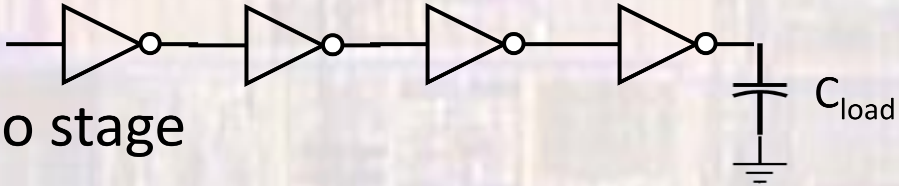
Digital Circuit Timing

- Driving a Large Capacitive Load
  - Clk signals
  - Long wires
  - External circuitry



Digital Circuit Timing

- Driving a Large Capacitive Load
  - N – number of stages
  - s – scale factor from stage to stage
  - C_{inv} – base inverter input capacitance
  - C_{load} – load capacitance
  - γ – Ratio of an inverters output capacitance to input capacitance (Typically ≤ 1)
  - t_{p0} – base inverter delay

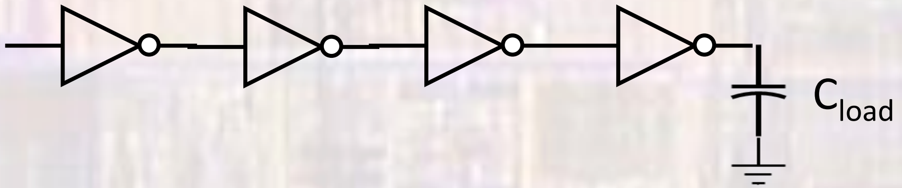


$$s = \sqrt[N]{C_{load}/C_{inv}}$$

$$t_{pd} = N t_{p0}\left(1 + \frac{\sqrt[N]{C_{load}/C_{inv}}}{\gamma}\right)$$

Digital Circuit Timing

- Driving a Large Capacitive Load
  - How many stages?



$$s_{opt} = exp\left(1 + {}^{\gamma}/_{s_{opt}}\right)$$

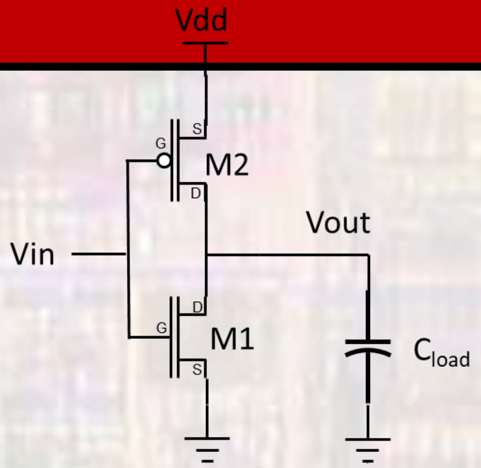
  - Only has an analytic solution for $\gamma = 0$

$$s_{opt} = e = 2.718 \qquad N_{opt} = ln\left({}^{C_{load}}/_{C_{inv}}\right)$$

  - For the more realistic value of $\gamma = 1$

$$s_{opt} \approx 3.6 \qquad N_{opt} = log_{3.6}\left({}^{C_{load}}/_{C_{inv}}\right)$$

C-MOS Circuits



- Power
  - DC power
    - Junction leakage (S/D to Body)
      - Becomes important for large designs
      - Power ∝ Vdd
  - Switching Power
    - Charging / Dis-charging the load

$$E = \int_0^\infty i(t)V_{out}dt = \int_0^\infty C\frac{dv}{dt}V_{out}dt = \int_0^{V_{dd}} CV_{out}dv = \frac{1}{2}CV_{dd}^2$$

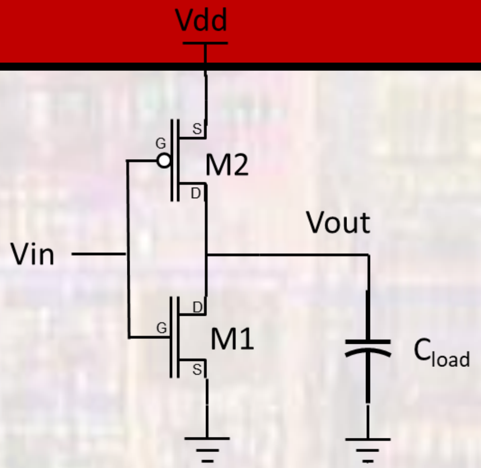
- Rising and falling

$$E = CV_{dd}^2$$

Power is a sq function of Vdd

$$P = CV_{dd}^2 F$$

C-MOS Circuits



- Power
  - Shoot-Through
    - Short period of time when both devices are on
    - Current from Vdd to Gnd
    - Can cause noise in Vdd and Gnd

$$P = I_{peak}V_{dd}\left(\frac{t_r + t_f}{2}\right)F$$

  - Total power
    - α – proportion of clock intervals actually switching
    - β – leakage factor

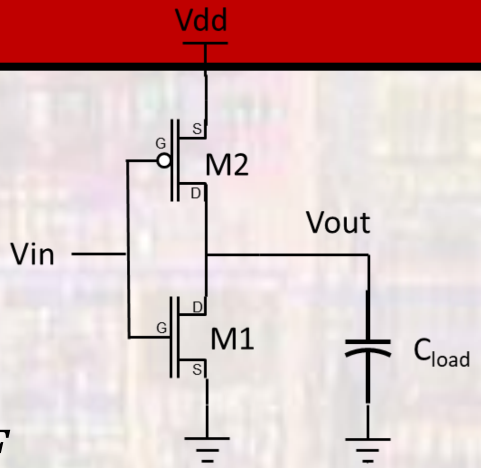
$$P = P_{DC} + P_{SW} + P_{Shoot}$$

All terms a function of Vdd

$$P = \beta V_{DD} + \alpha C V_{dd}^2 F + \alpha I_{peak}V_{dd}\left(\frac{t_r + t_f}{2}\right)F$$

C-MOS Circuits

- Power – Speed Tradeoff



$$P = \beta V_{DD} + \alpha C V_{dd}^{2} F + \alpha I_{peak} V_{dd} \left(\frac{t_r + t_f}{2}\right) F$$

$$t_{pd} = \frac{C_{load}\, V_{dd}}{\frac{k'_n}{2} \frac{W}{L} (V_{dd} - V_t)^2}$$

Power goes up as Vdd^3 when optimizing for peak speed