# C-MOS Circuits

Last updated 4/10/22

# C-MOS Circuits

- Parameters $K_n = \frac{W\mu_n C_{ox}}{2L}$ $K_p = \frac{W\mu_p C_{ox}}{2L}$

$K_n = \frac{k'_n}{2}\frac{W}{L}$ $k'_n = \mu_n C_{ox}$ $K_p = \frac{k'_p}{2}\frac{W}{L}$ $k'_p = \mu_p C_{ox}$

$\mu_n,\ \mu_p, C_{ox}$ fixed for a given semiconductor process →

$k'_n$ , $k'_p$ fixed for a given semiconductor process

$I_D = K_n[2(V_{GS} - V_{tn})V_{DS} - V_{DS}^2]$

$I_D = \frac{k'_n}{2}\frac{W}{L}[2(V_{GS} - V_{tn})V_{DS} - V_{DS}^2]$

$I_D = K_p[2(V_{SG} - V_{tp})V_{SD} - V_{SD}^2]$

$I_D = \frac{k'_p}{2}\frac{W}{L}[2(V_{SG} - V_{tp})V_{SD} - V_{SD}^2]$

$V_{DSsat} = V_{GS} - V_{th}$

$I_D = K_n(V_{GS} - V_{tn})^2$

$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_{tn})^2$

$C_{Gn} = W \times L \times {}^{k'_n}/_{\mu_n}$

$V_{SDsat} = V_{SD} - V_{th}$

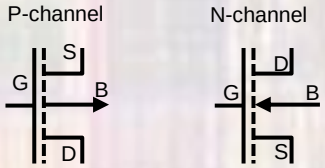
$I_D = K_p(V_{SG} - V_{tp})^2$

$I_D = \frac{k'_p}{2}\frac{W}{L}(V_{SG} - V_{tp})^2$

$C_{Gp} = W \times L \times {}^{k'_p}/_{\mu_p}$

# C-MOS Circuits

- Enhancement Mode
  - A bias is required to form the channel
  - 4-terminal symbol



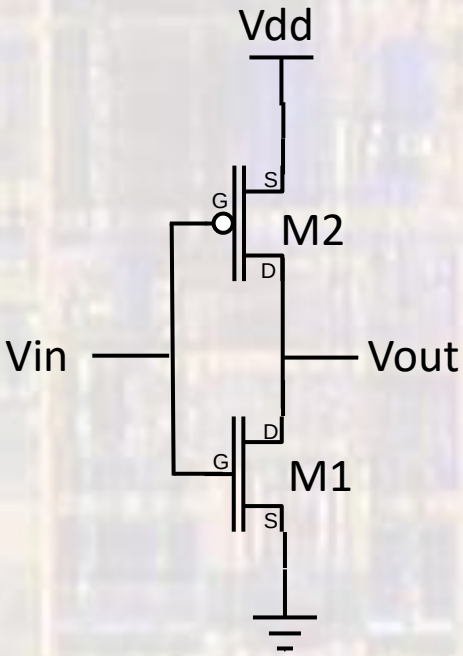

  - In digital applications the Source is typically tied to
    - Vdd for P-MOS
    - Gnd for N-MOS


  - The simplified logic symbols


Note – almost all N-MOS and P-MOS devices used today are enhancement mode – so the dashed line is omitted

# C-MOS Circuits

- Inverter - Design




Assuming Vdd is big enough to keep M2 and M1 in saturation at the switching point

$$\frac{k'_p}{2}\frac{W2}{L2}\left(V_{sg2}-V_{tp}\right)^2=\frac{k'_n}{2}\frac{W1}{L1}\left(V_{gs1}-V_{tn}\right)^2$$

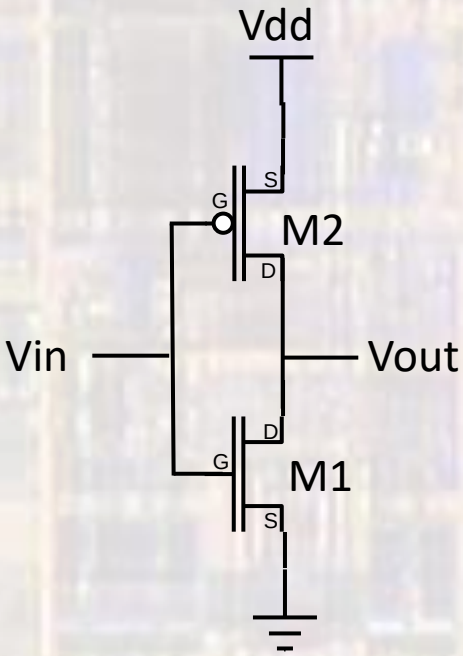
Desire a consistent switching point Vin = Vout = Vdd/2

$$\frac{k'_p}{2}\frac{W2}{L2}\left(V_{dd}/2-V_{tp}\right)^2=\frac{k'_n}{2}\frac{W1}{L1}\left(V_{dd}/2-V_{tn}\right)^2$$

$$\frac{W1/L1}{W2/L2}=\frac{k'_p}{k'_n}\left(\frac{V_{dd}/2-V_{tp}}{V_{dd}/2-V_{tn}}\right)^2$$

# C-MOS Circuits

- Inverter - Design




Desire a consistent switching point Vin = Vout = Vdd/2

$$\frac{W1/_{L1}}{W2/_{L2}} = \frac{k'_p}{k'_n}\left(\frac{V_{dd}/2 - V_{tp}}{V_{dd}/2 - V_{tn}}\right)^2$$

If we make $V_{tp} = V_{tn}$, $V_{dd}$ drops out of the equation

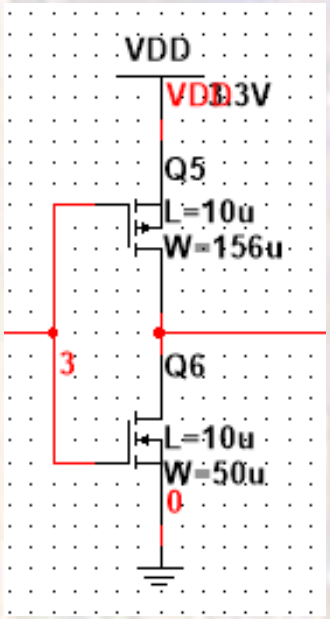
$$\frac{W1/_{L1}}{W2/_{L2}} = \frac{k'_p}{k'_n}$$

And the switching point remains $V_{dd}/2$ regardless of $V_{dd}$**

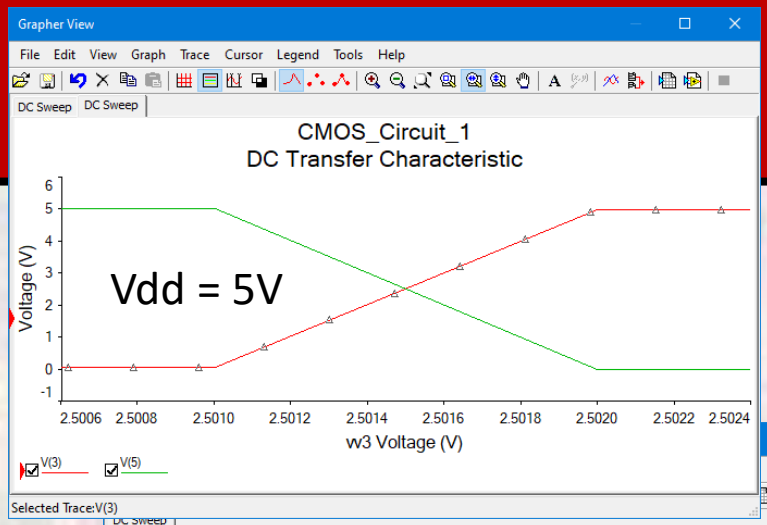
** as long as both devices are in saturation

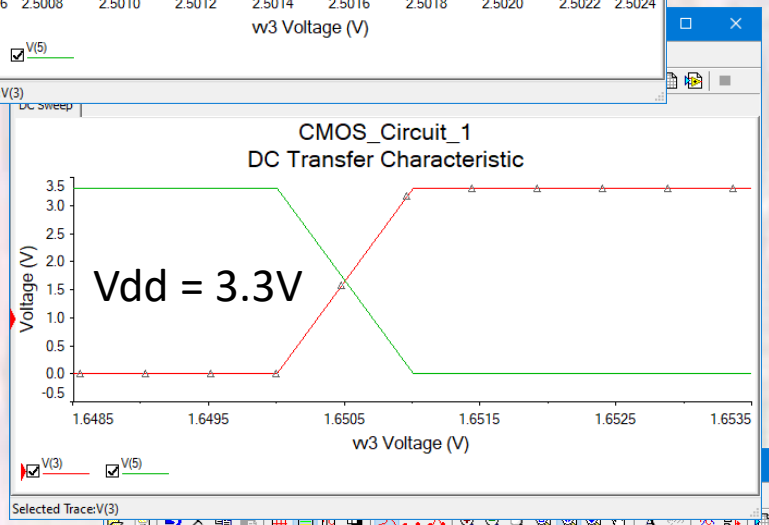
# C-MOS Circuits

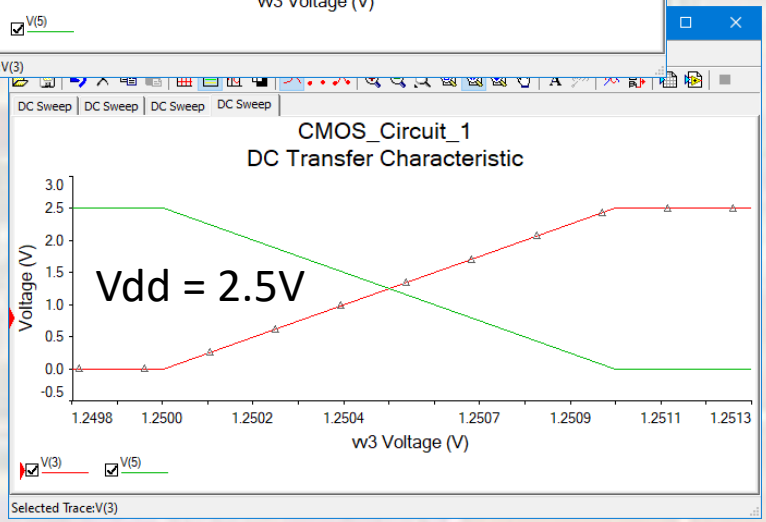
- Inverter - Design




Vt = 1V
Vtn = 1V
Vtp = -1V (1V)
k'n = 14uA/V$^2$
k'p = 4.5uA/V$^2$

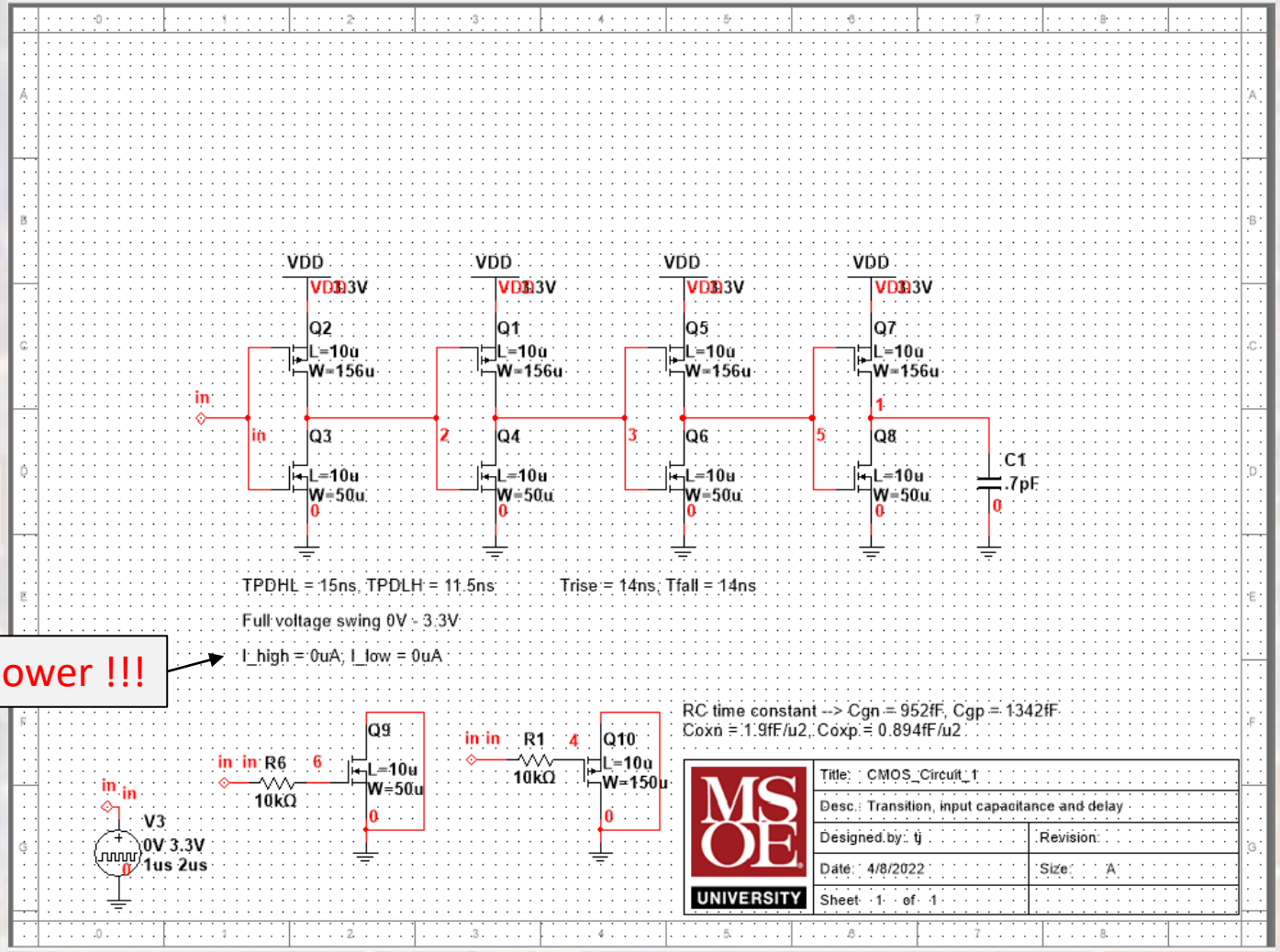


# C-MOS Circuits

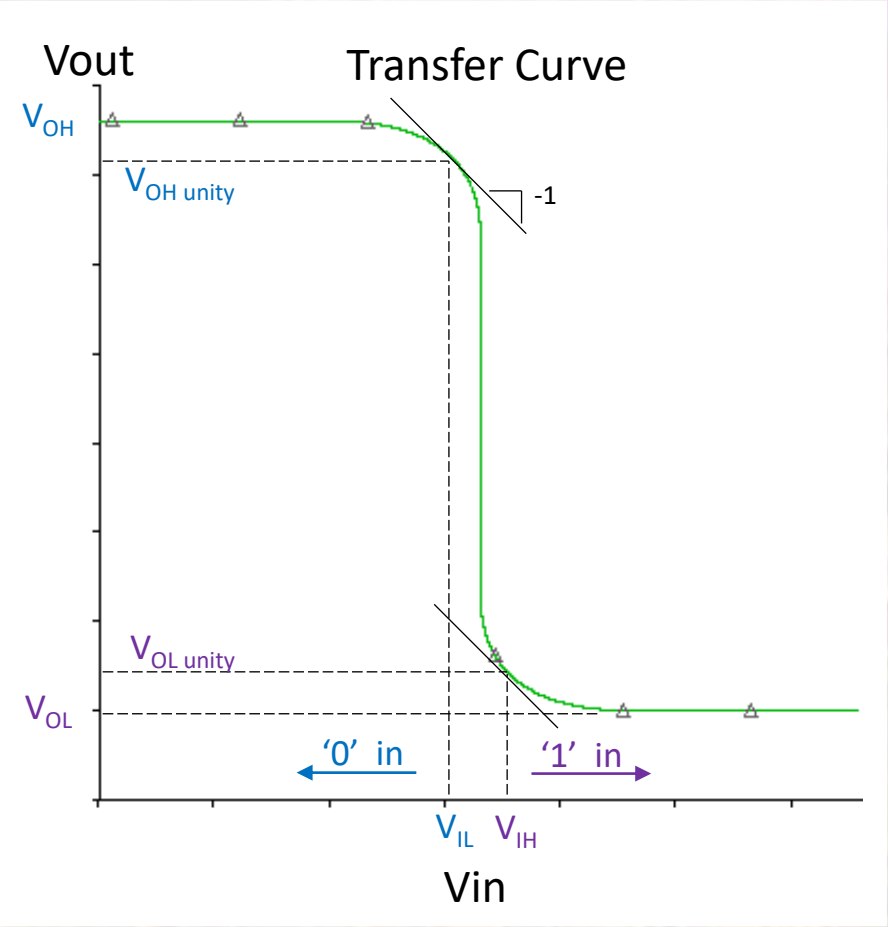
- Inverter - Design




No DC power !!!

# C-MOS Circuits

- Inverter - Design




$V_{OL}$ : Maximum output voltage that will be considered a low

$V_{OH}$ : Minimum output voltage that will be considered a high

$V_{IL}$ : Maximum input voltage that will result in a high output voltage

$V_{IH}$ : Minimum input voltage that will result in a low output voltage

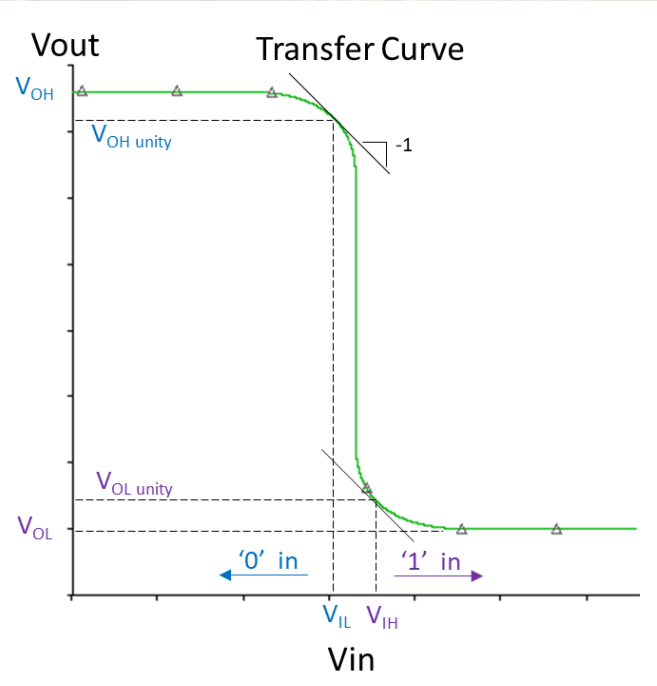
Noise Margin (NM) : The amount of noise in the input signals that the system can tolerate without causing the output to change when it shouldn't

$NM_L = V_{IL} - V_{OL\ unity}$

$NM_H = V_{OH\ unity} - V_{IH}$

# C-MOS Circuits

- Inverter - Design




$$V_{IL(K_n=K_p)} = V_{tn} + \frac{3}{8}(V_{DD} + V_{tp} - V_{tn})$$

$$V_{IH(K_n=K_p)} = V_{tn} + \frac{5}{8}(V_{DD} + V_{tp} - V_{tn})$$

$$V_{OL\ unity(K_n=K_p)} = \frac{1}{2}(2V_{IH} - V_{DD} - V_{tp} - V_{tn})$$

$$V_{OH\ unity(K_n=K_p)} = \frac{1}{2}(2V_{IL} + V_{DD} - V_{tp} - V_{tn})$$

Vdd = 3.3V
Vtn = -Vtp = 1V
VIL = 1.488V, VIH = 1.813V
VOLunity = 160mV, VOHunity = 3.14V

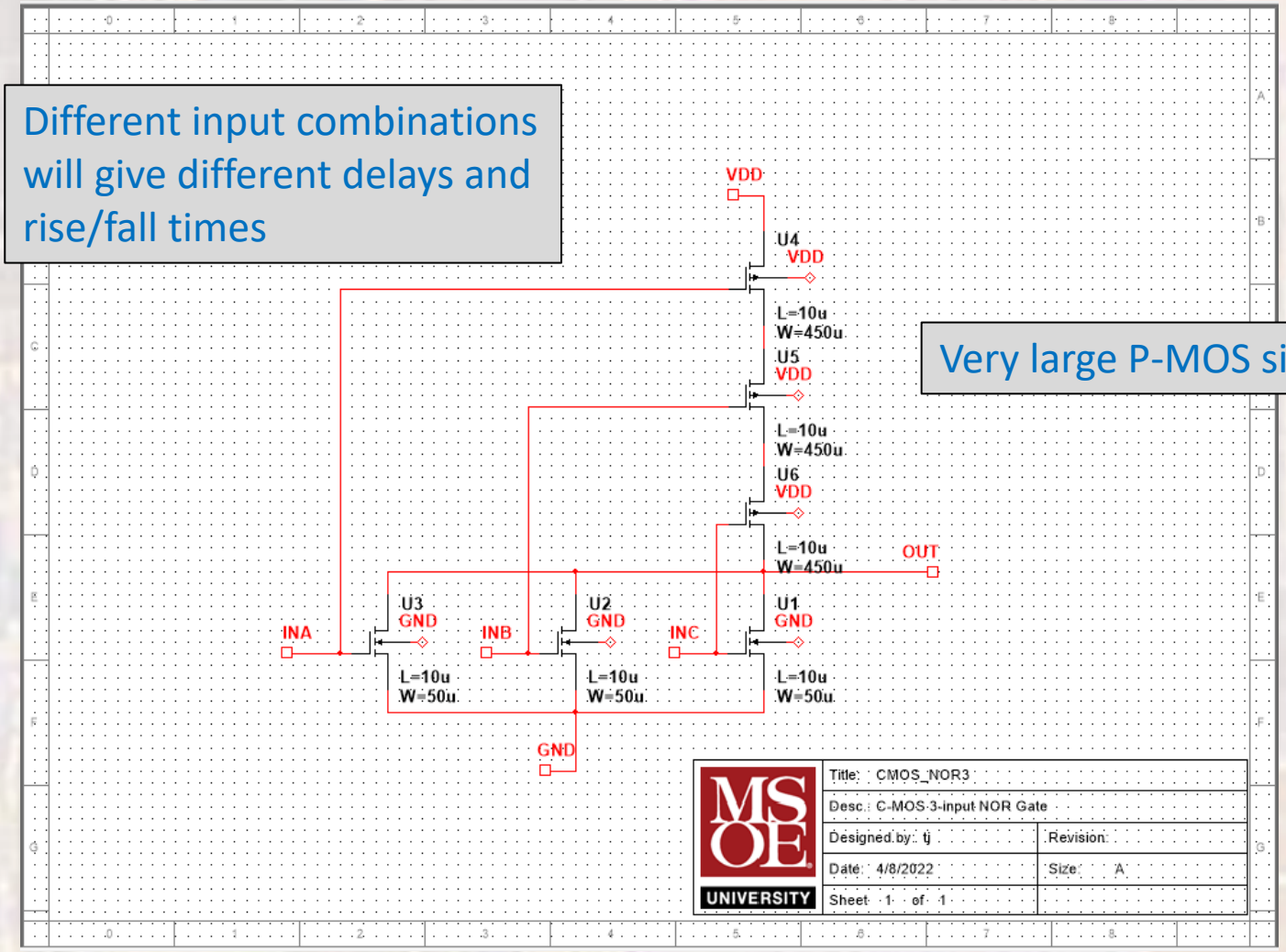
NML = 1.326V
NMH = 1.326V

$NM_L = V_{IL} - V_{OL\ unity}$

$NM_H = V_{OH\ unity} - V_{IH}$

# C-MOS Circuits

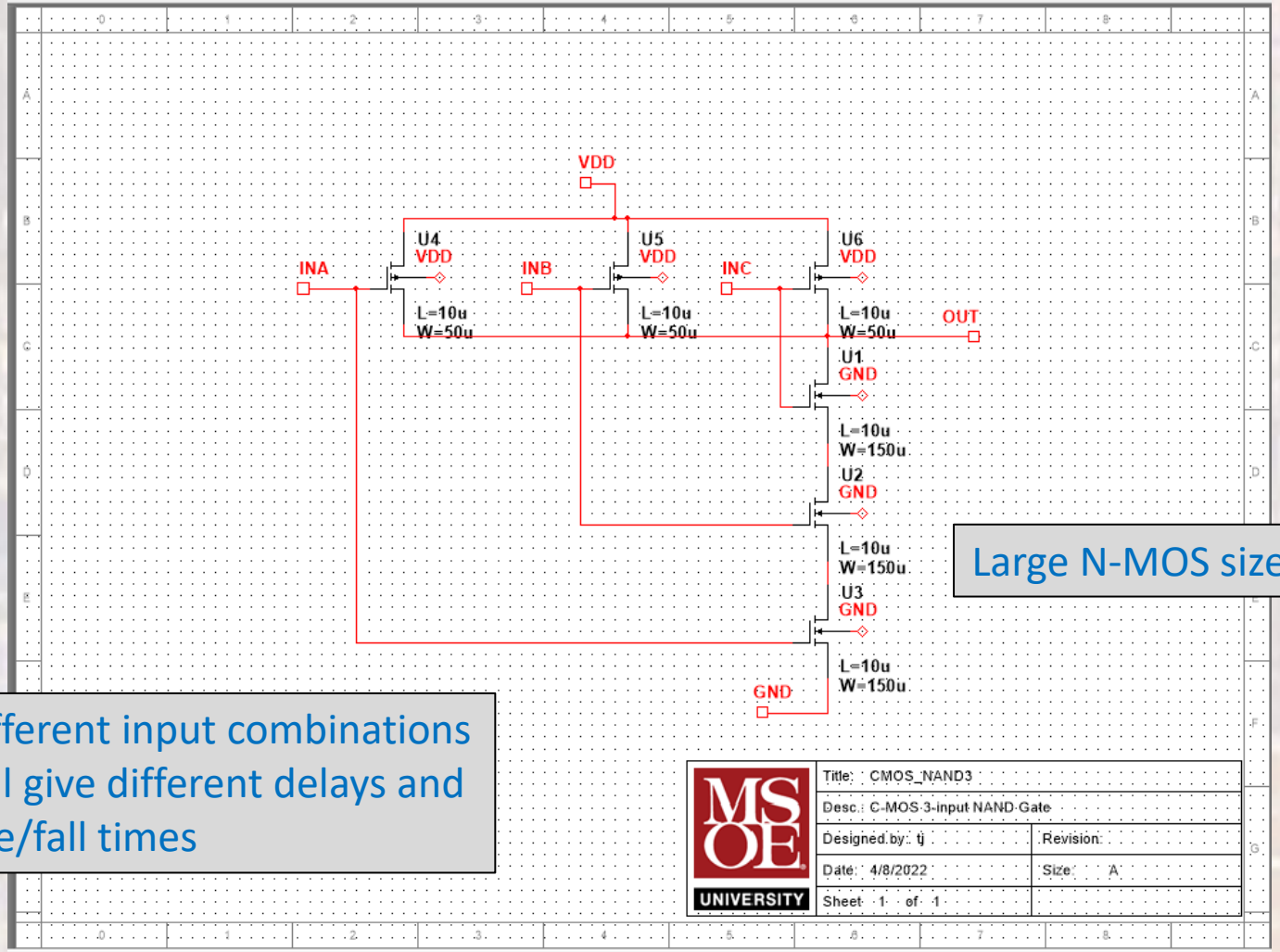
- C-MOS Gates



# C-MOS Circuits

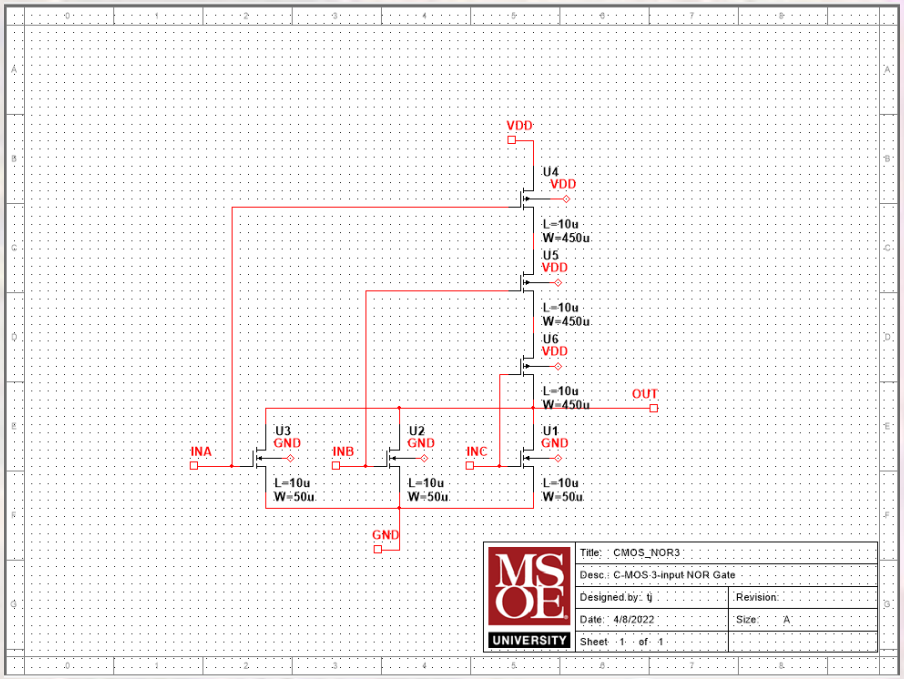
- C-MOS Gates

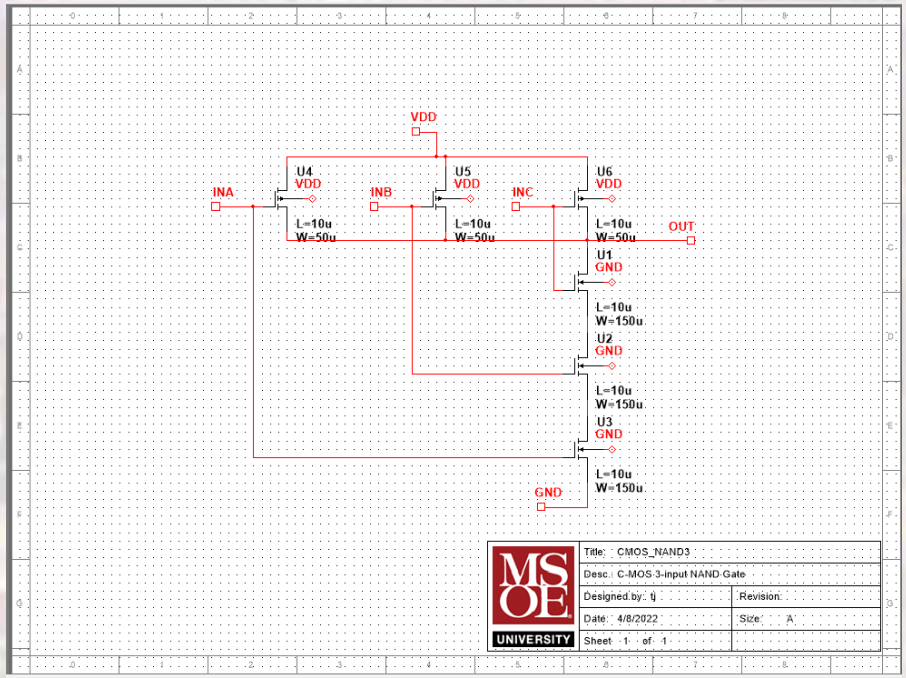


# C-MOS Circuits

- C-MOS Gates



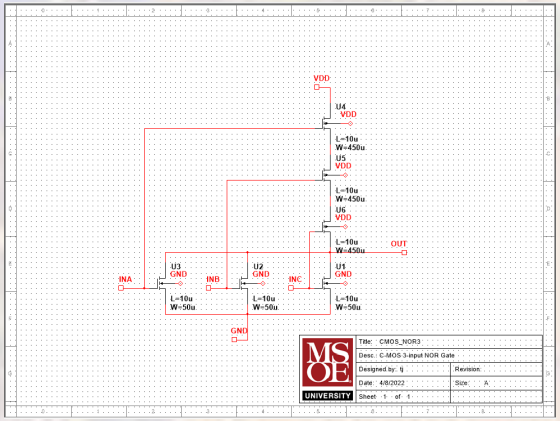

Total transistor gate area
$15{,}000u^2$

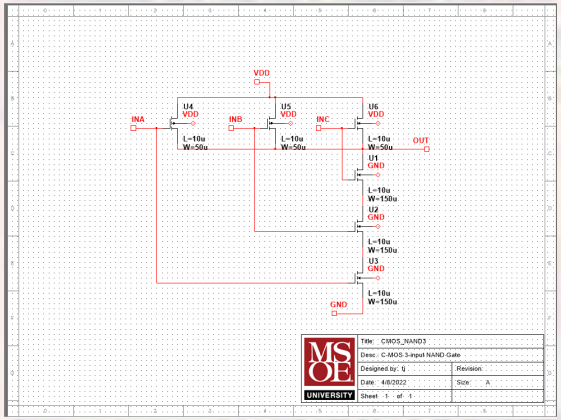
Total transistor gate area
$6{,}000u^2$

NAND gates preferred
over NOR gates

# C-MOS Circuits

- C-MOS Gates
  - Use a 2 input NAND gate as a reference for size and loading




Relative Size

2 input NAND gate area = 3000u$^2$ = 1 NAND equivalent

INV gate area = 1000u$^2$ = 1/3 NAND Eq.
2 input NOR gate area = 7000u$^2$ = 2.33 NAND Eq.
3 NAND = 2 NAND eq.
4 NAND = 3.33 NAND eq.
3 NOR = 5 NAND eq.
4 NOR = 8.66 NAND eq.

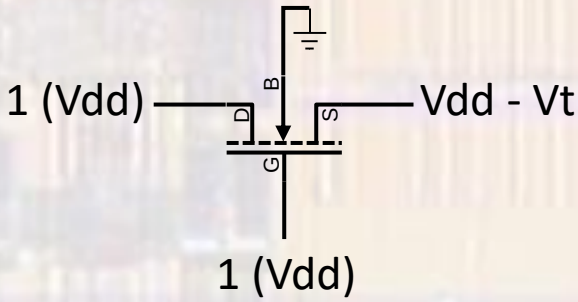
Input Load (relative capacitance – 1 input)

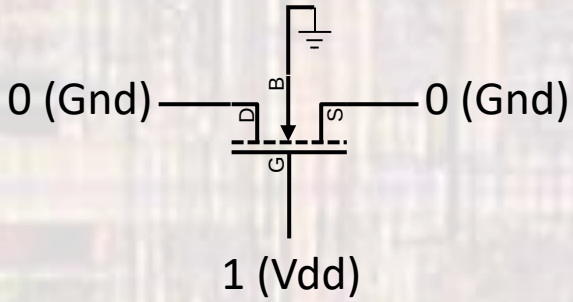
2 input NAND gate area/input = 1500u$^2$ = 1 NAND equivalent

INV gate area/input = 1000u$^2$ = 2/3 NAND Eq.
2 input NOR gate area/input = 4000u$^2$ = 2.33 NAND Eq.
3 NAND/input = 1.33 NAND eq.
4 NAND/input = 1.66 NAND eq.
3 NOR/input = 3.33 NAND eq.
4 NOR/input = 4.33 NAND eq.

# C-MOS Circuits

- N-MOS Transmission Gates
  - Use a single N-MOS device as a “pass gate”
    - Passes a ‘0’
    - Reduced value for a ‘1’
    - Bi-directional

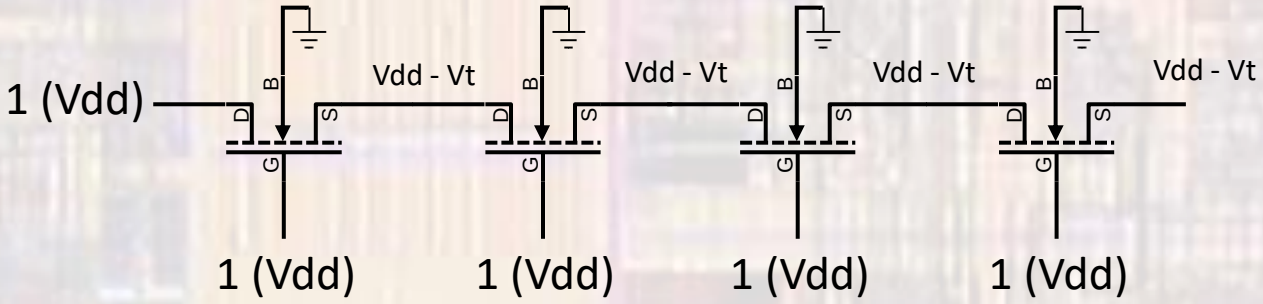


# C-MOS Circuits

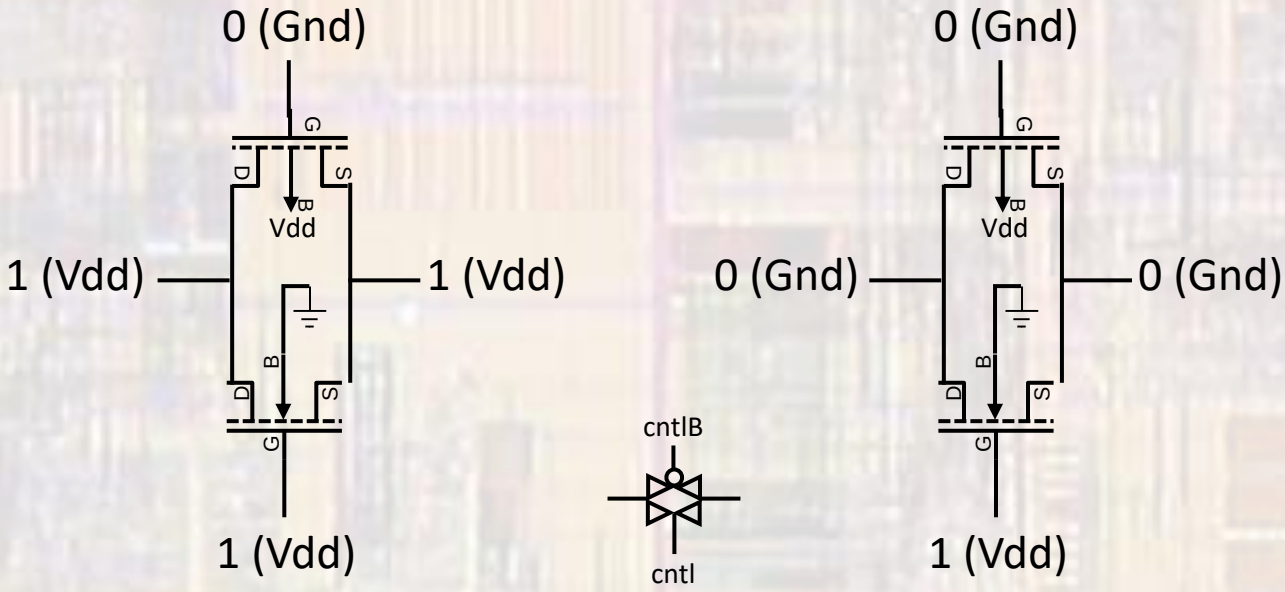
- N-MOS Transmission Gates
  - Chained N-MOS device as a “pass gate”
    - Passes a ‘0’
    - Reduced value for a ‘1’, but no further reduction
    - Multiplexer



# C-MOS Circuits

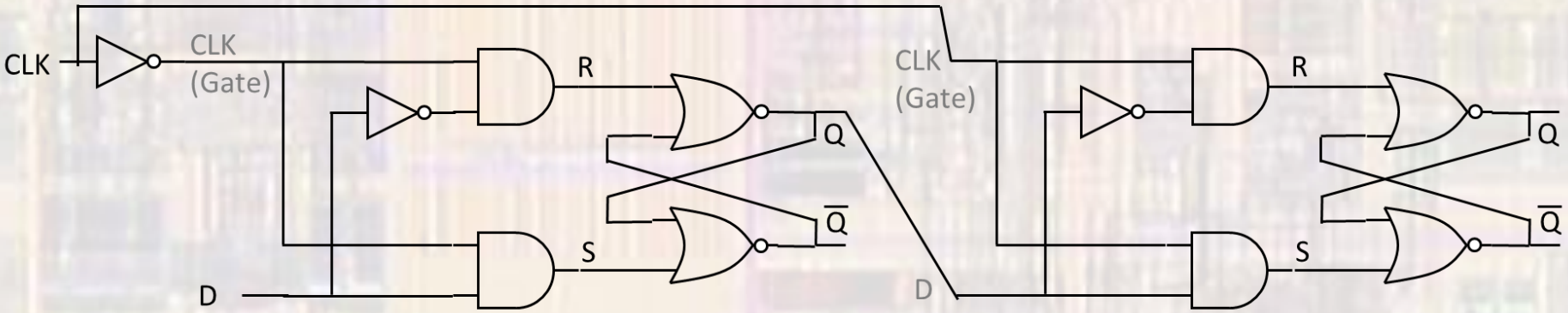
- C-MOS Transmission Gates
  - Use parallel P-MOS and N-MOS devices as a “pass gate”
    - Passes both ‘0’s and ‘1’s
    - Bi-directional
    - Requires cntl and cntlB



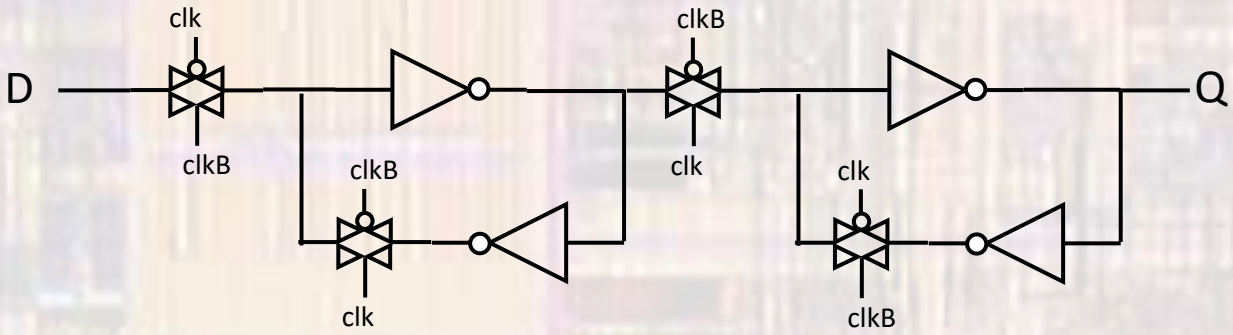
# C-MOS Circuits

- C-MOS Flip-Flop
  - Logical Circuit
    - 2, SR latches



# C-MOS Circuits

- C-MOS Flip-Flop
  - Common Circuit



# C-MOS Circuits

- C-MOS Tristate Inverter
  - Common Circuit