Emitter Coupled Logic Basics

Last updated 3/8/22

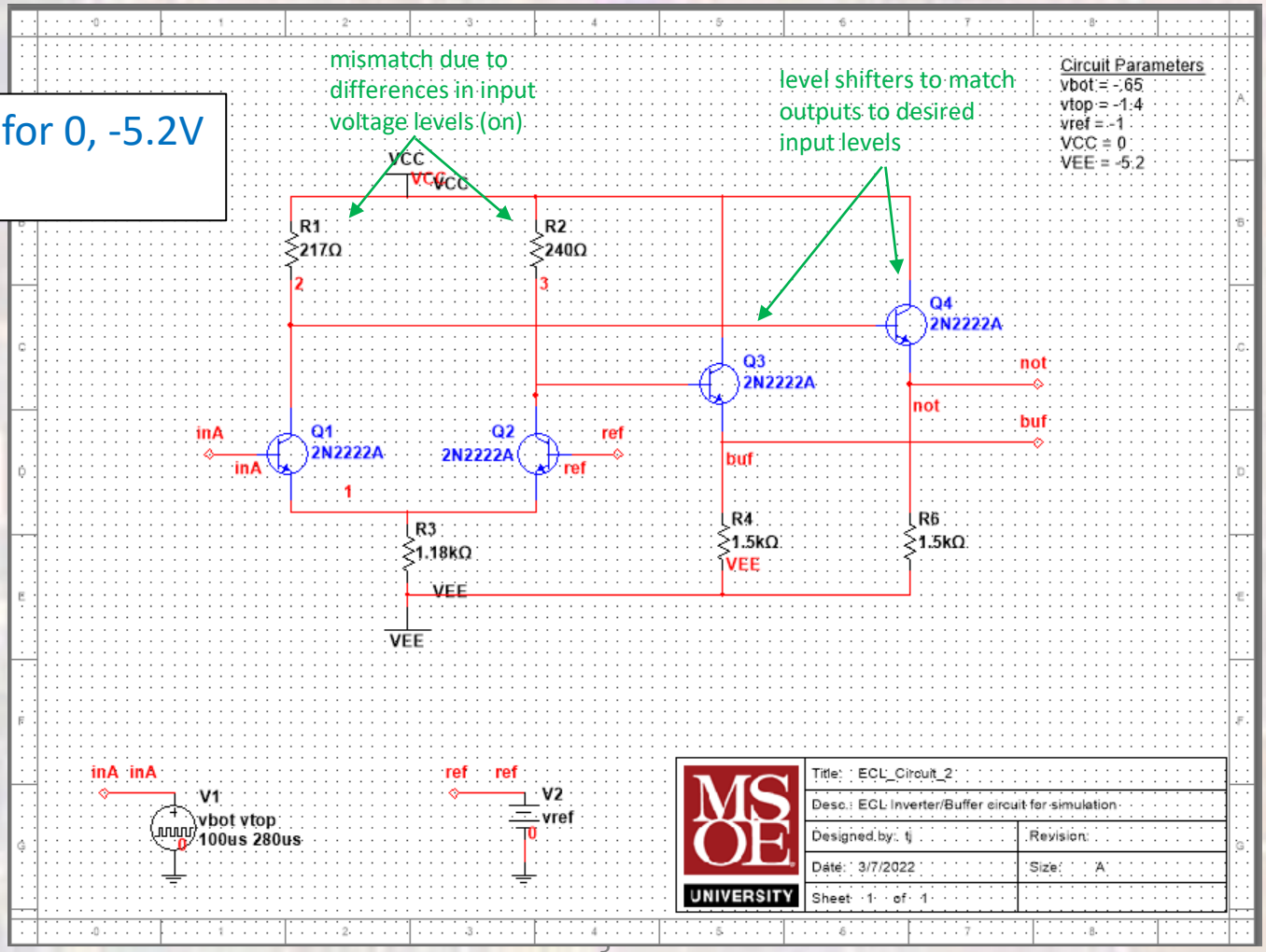
Emitter Coupled Logic - Basics

- History
  - Invented by IBM in the 1950s
  - High Speed logic solution of the 60s and 70s
  - Due to power concerns – used only where required
  - 500ps gate delays possible by the mid 70s
  - Replaced by NMOS and then CMOS in the 80s

Emitter Coupled Logic - Basics

- Inverter / Buffer Core Circuit

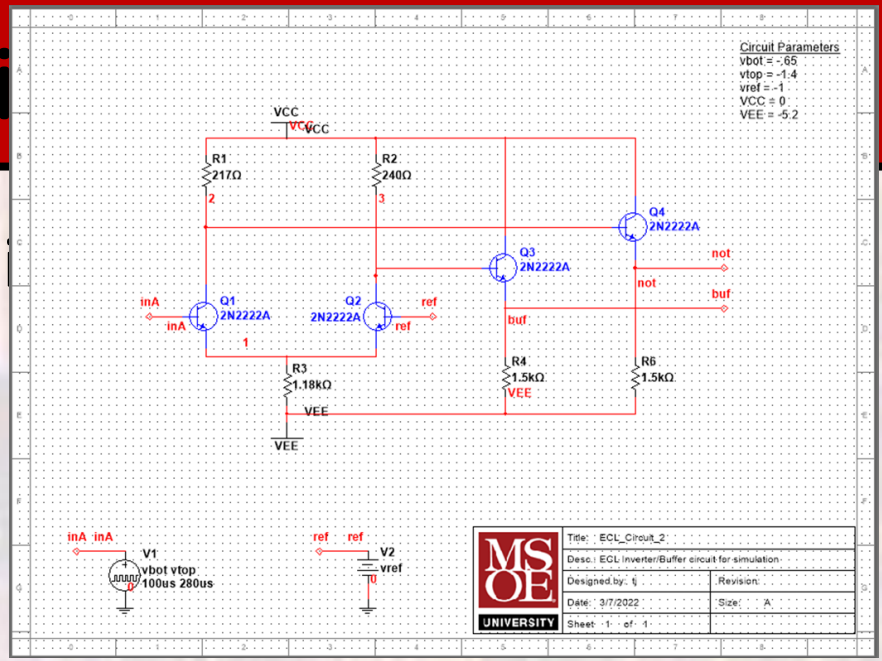
Configured for 0, -5.2V operation

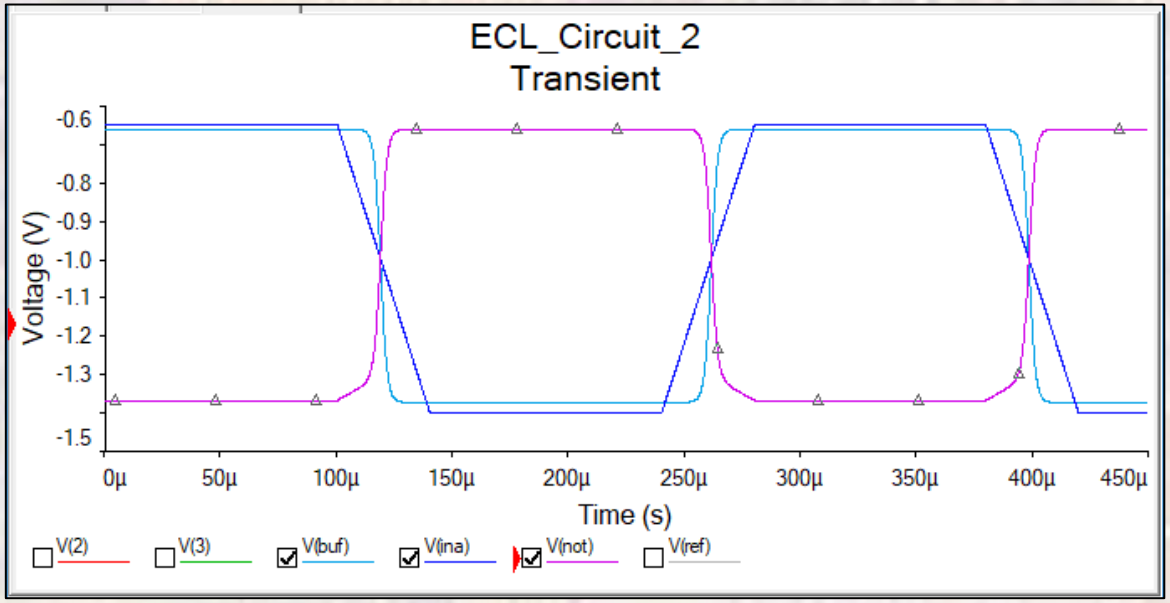


Emitter Coupled Logi

- Inverter / Buffer Core Circui
  - Low Speed
  - 0V, -5.2V

Note symmetric switching points





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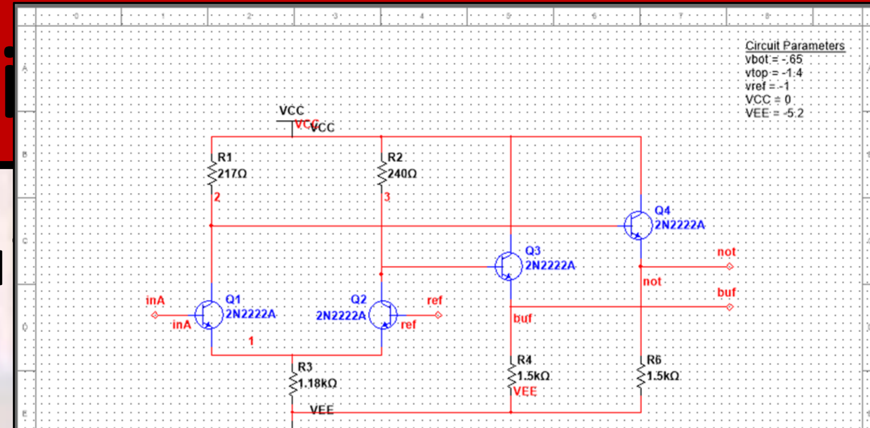
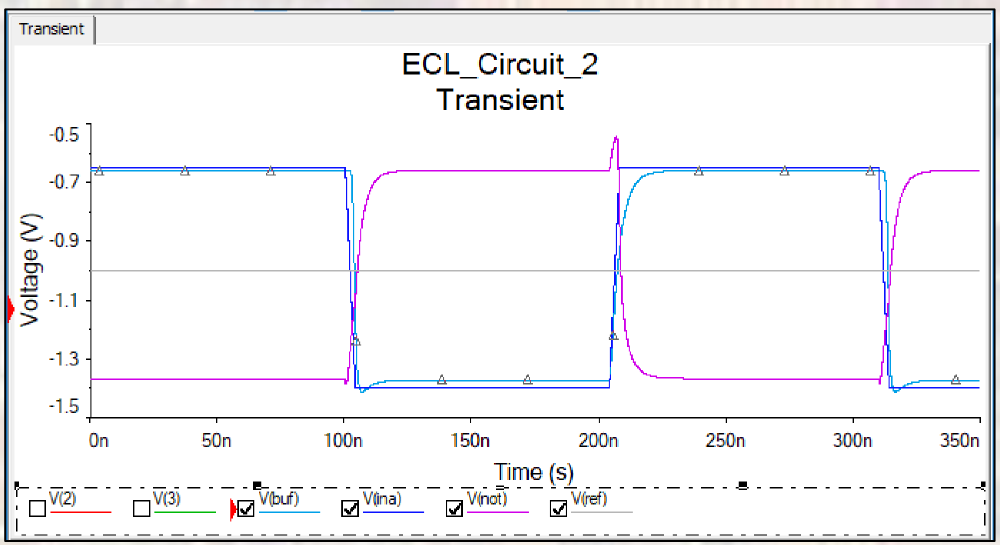
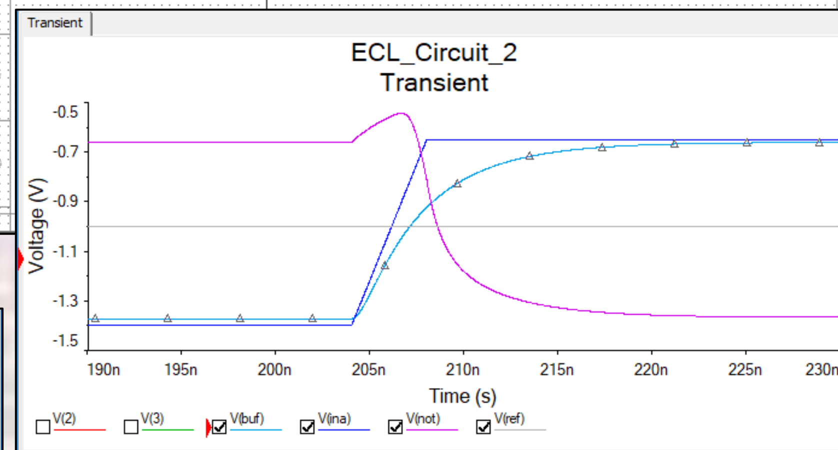
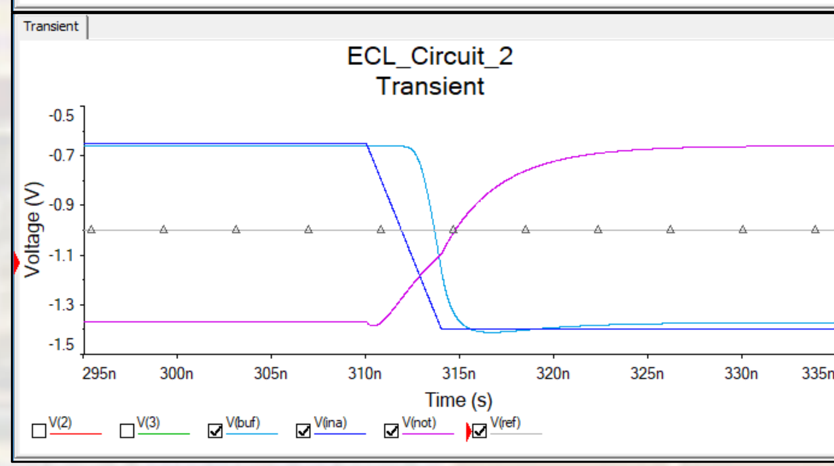
  - High speed switching
  - 0V, -5.2V

Why spikes on v(not) but not v(buf)?





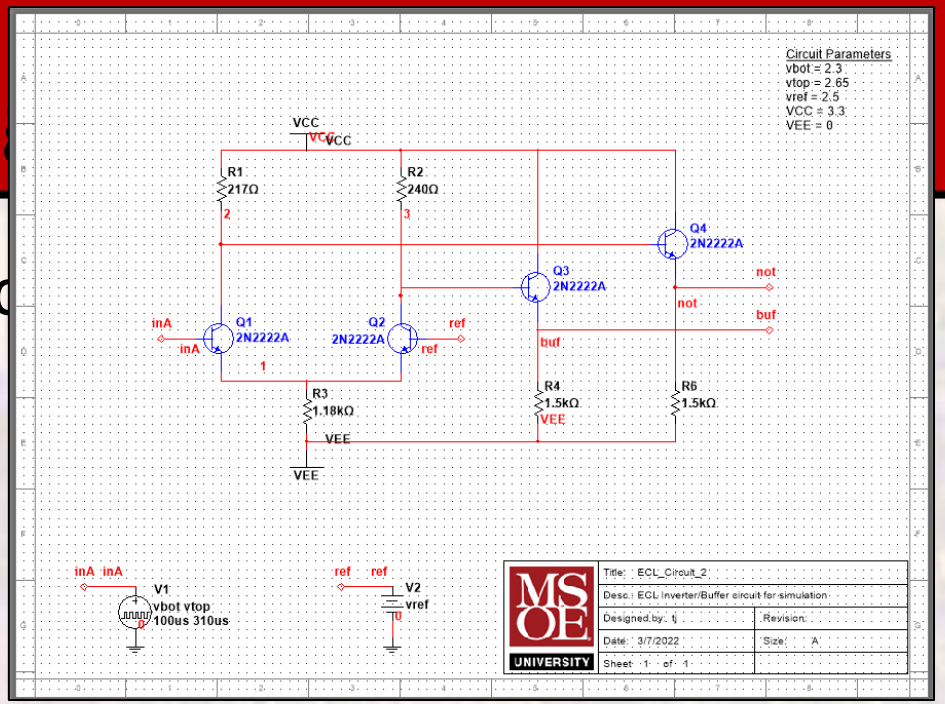


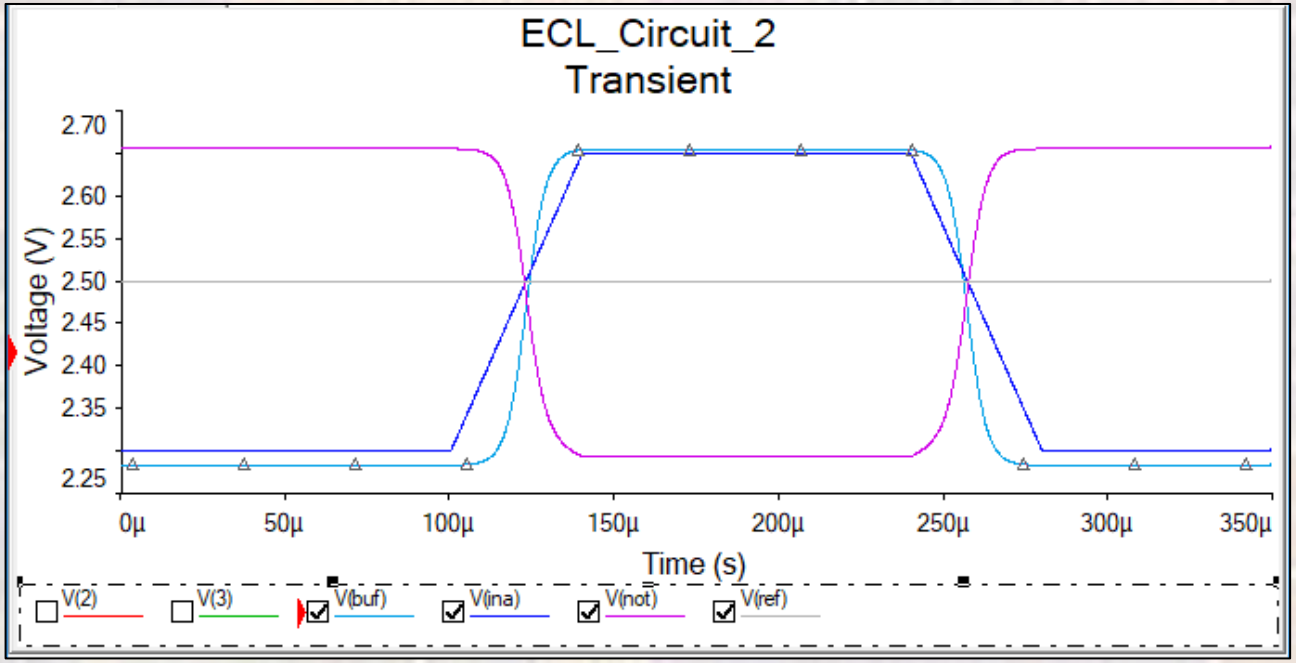


Emitter Coupled Lo

- Inverter / Buffer Core Circ
  - Low Speed
  - 3.3V, 0V
  - No circuit changes

Note symmetric switching points





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