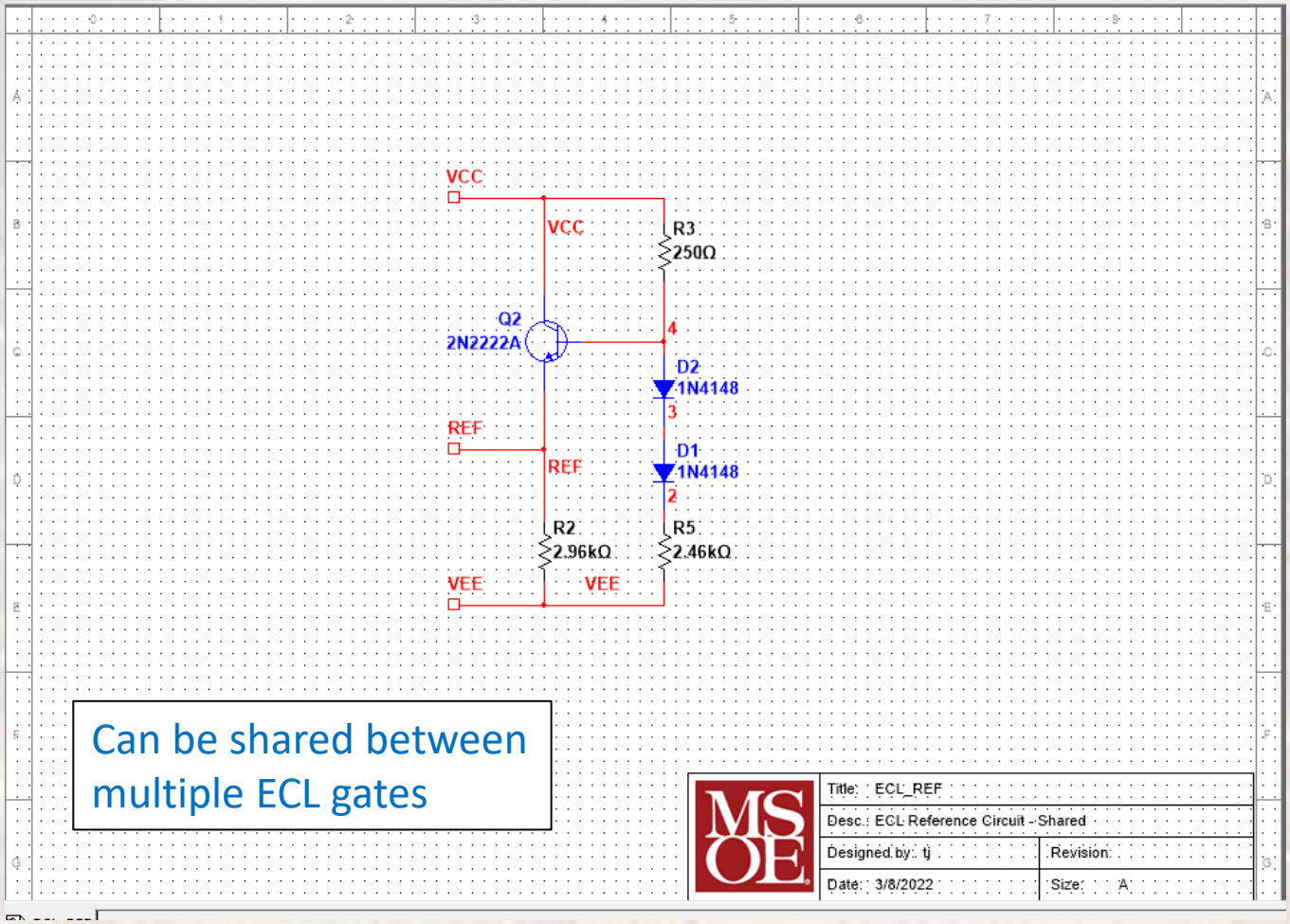
Emitter Coupled Logic Implementation

Last updated 3/8/22

Emitter Coupled Logic - Implementation

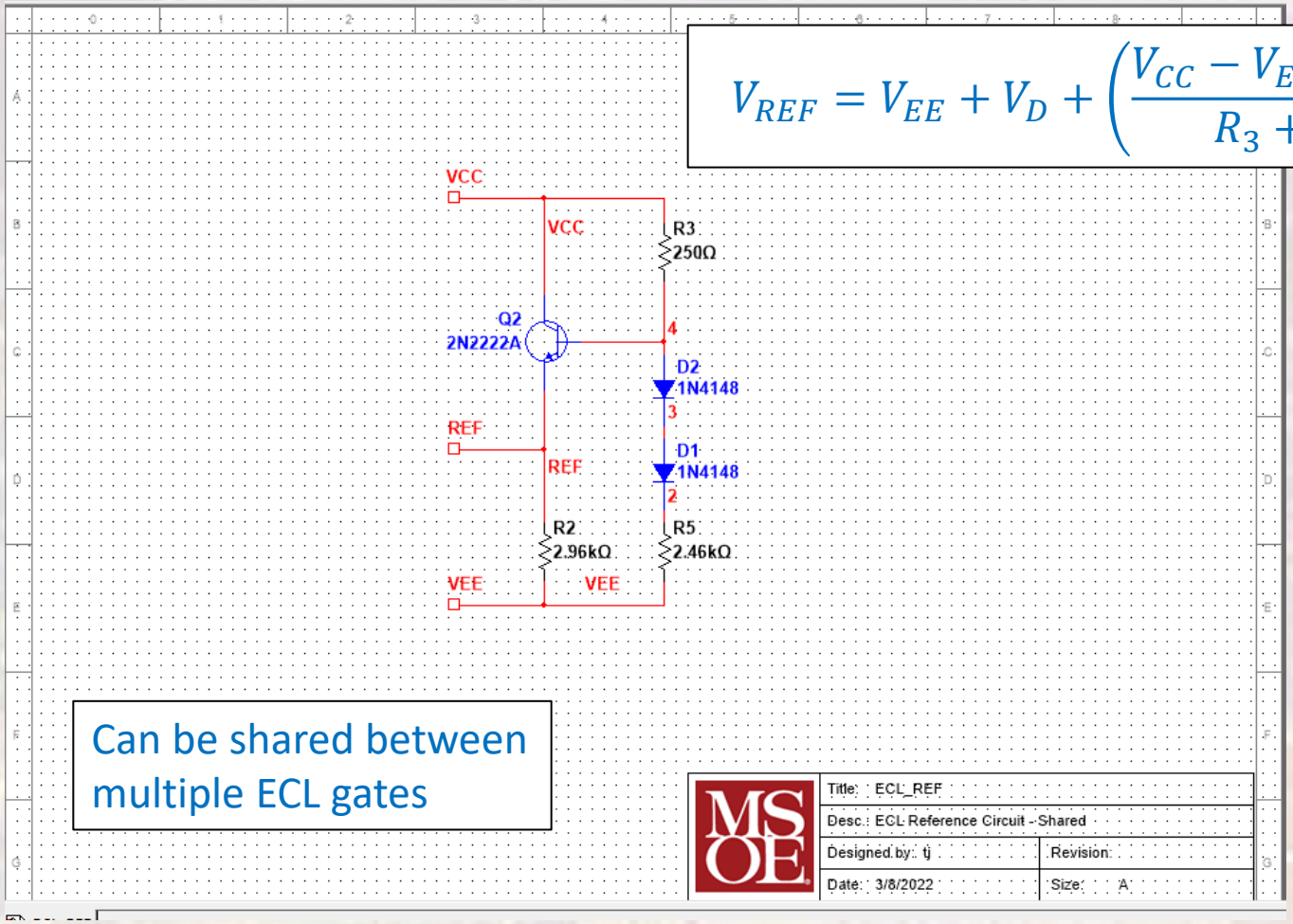
- Reference Generator



Emitter Coupled Logic - Implementation

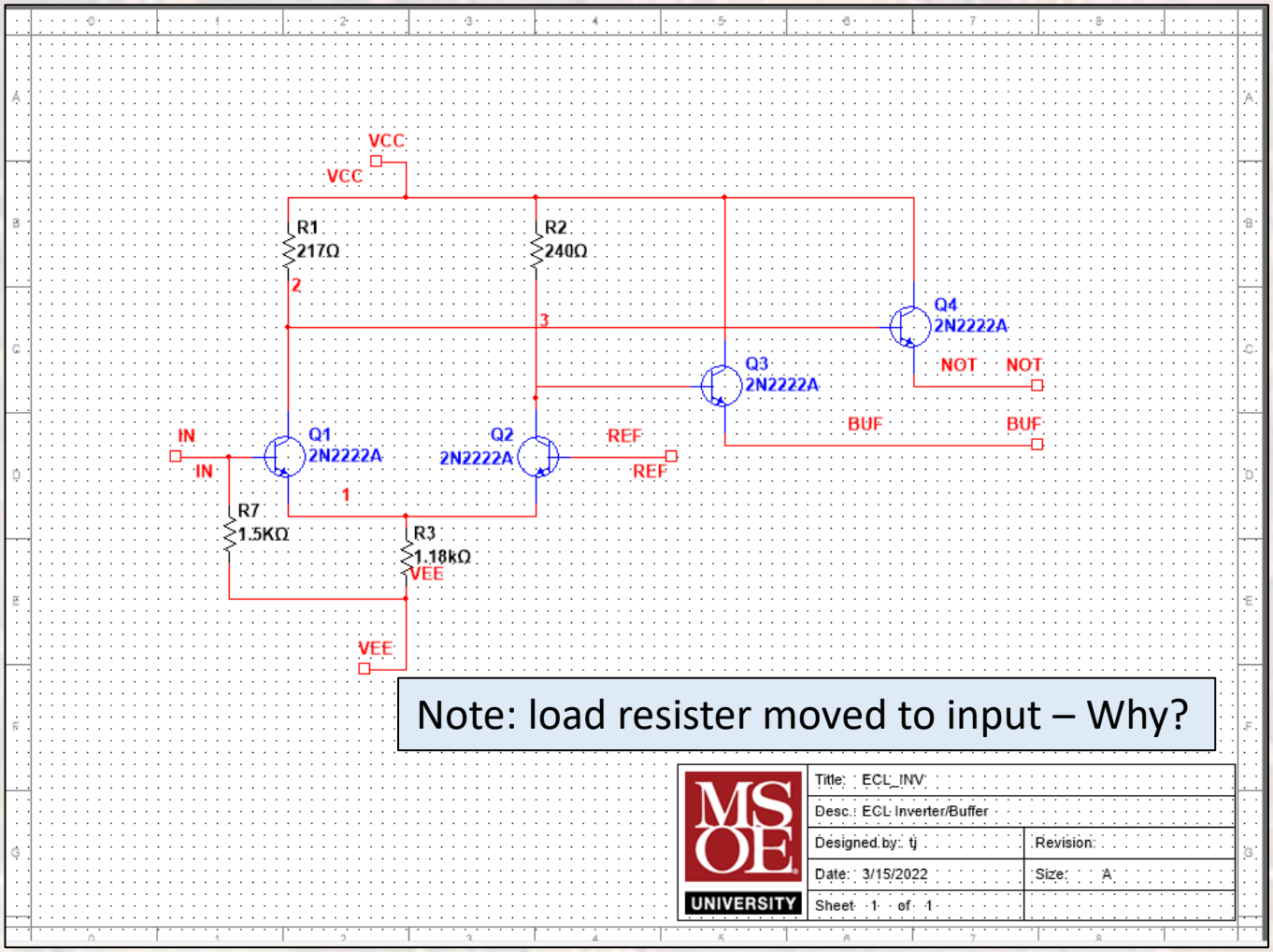
- Reference Generator

$$V_{REF} = V_{EE} + V_D + \left(\frac{V_{CC} - V_{EE} - 2V_D}{R_3 + R_5}\right) R_5$$



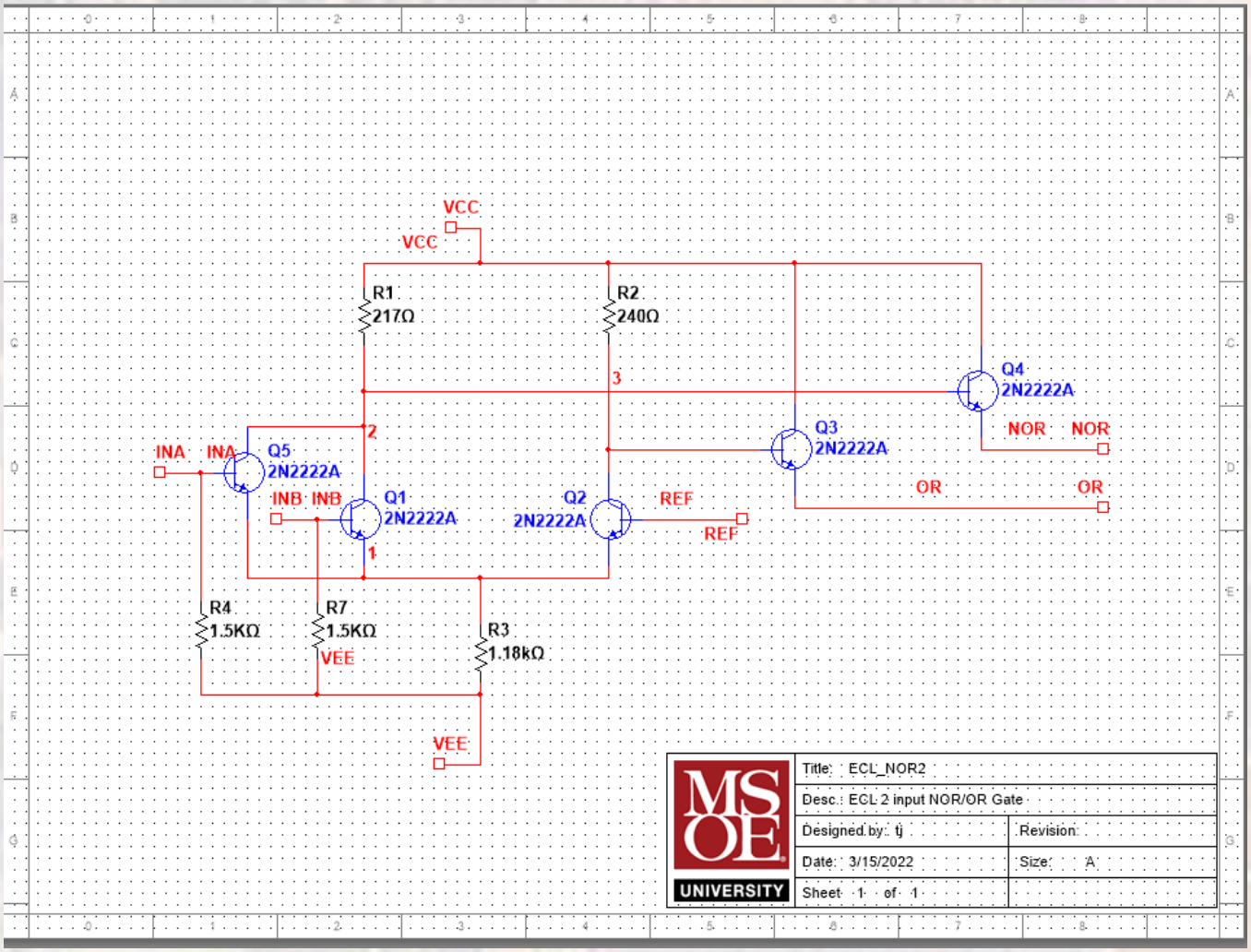
Emitter Coupled Logic - Implementation

- Inverter



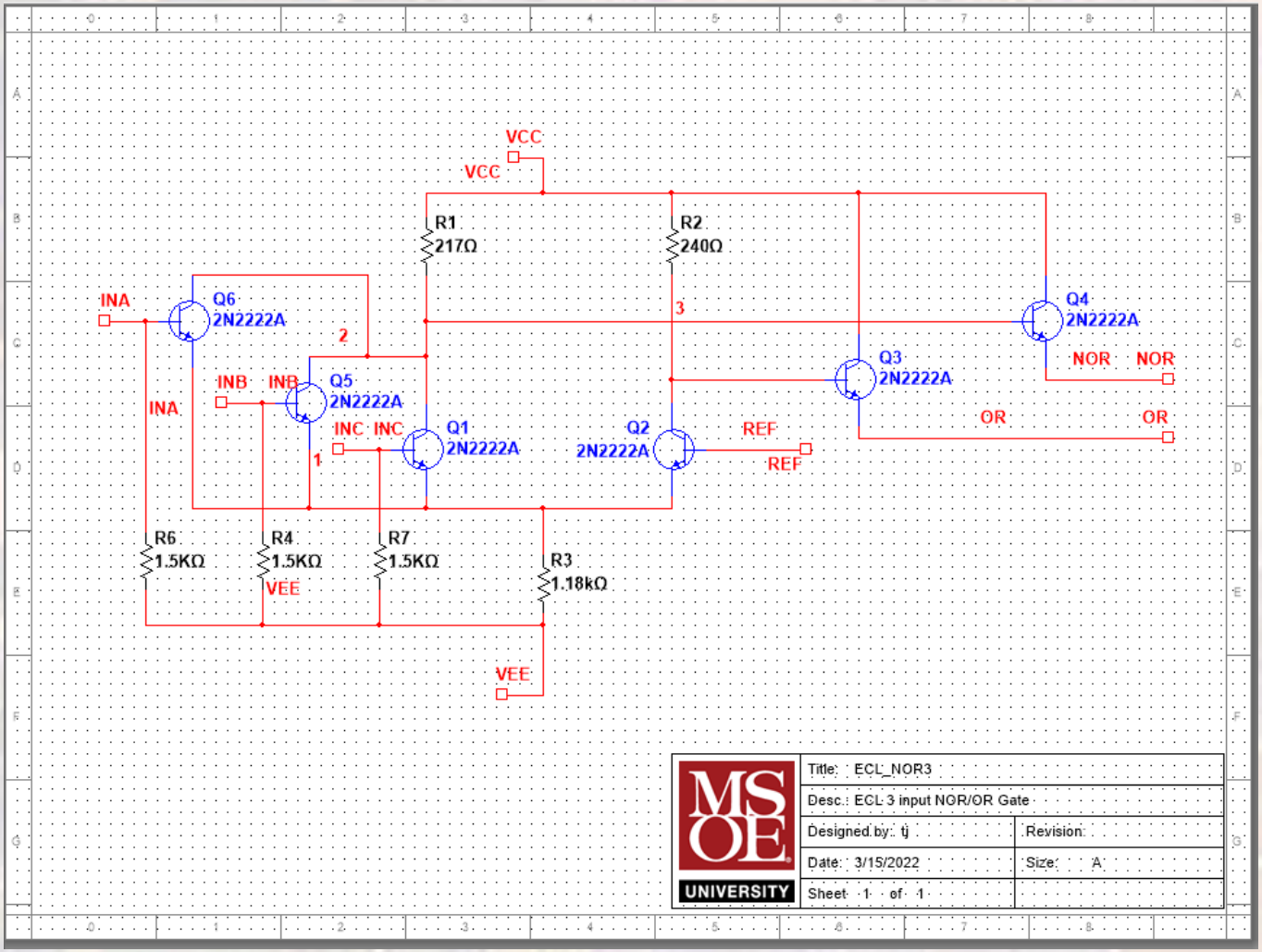
Emitter Coupled Logic - Implementation

- 2 Input NOR/OR



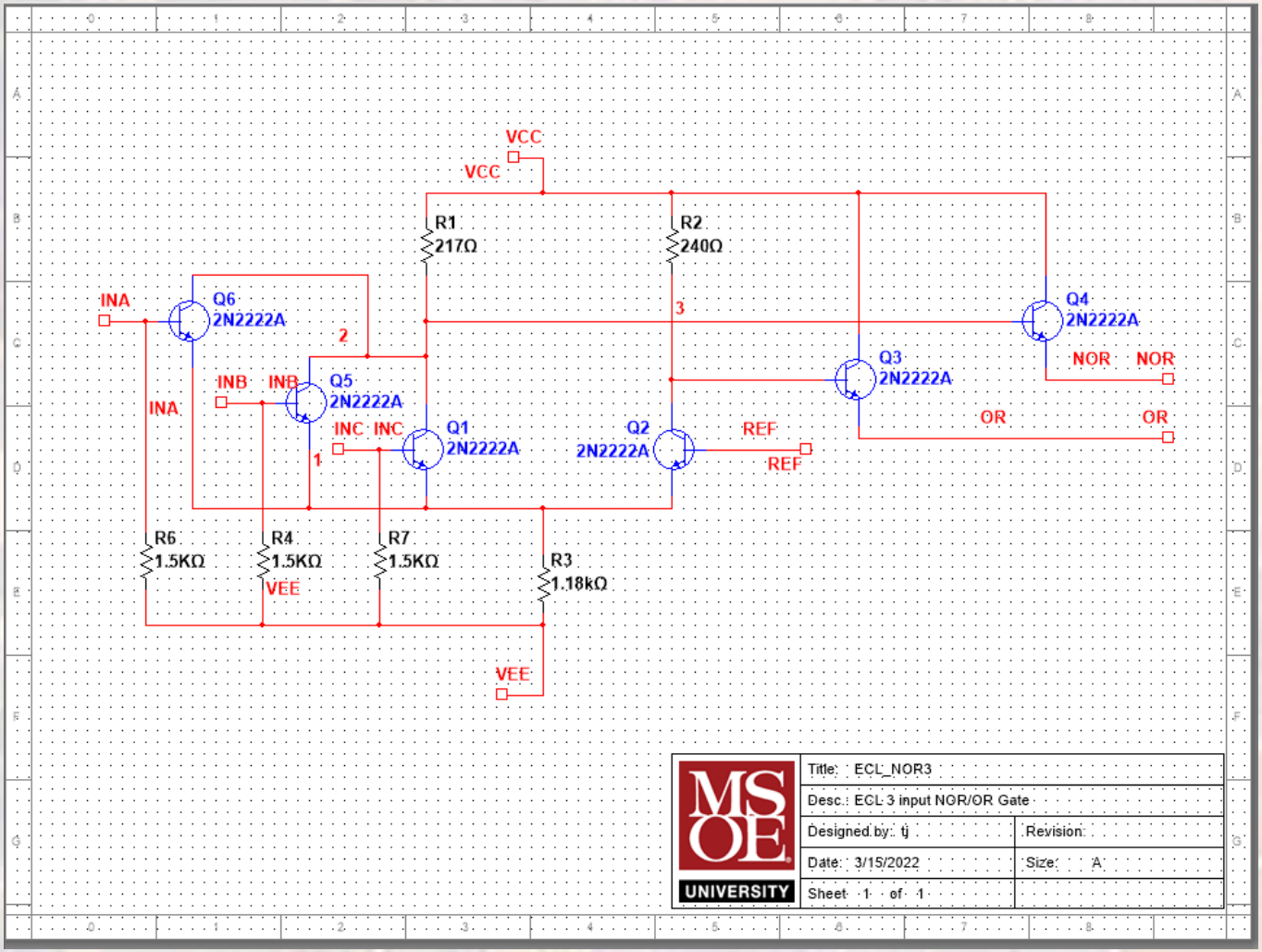
Emitter Coupled Logic - Implementation

- 3 Input NOR/OR



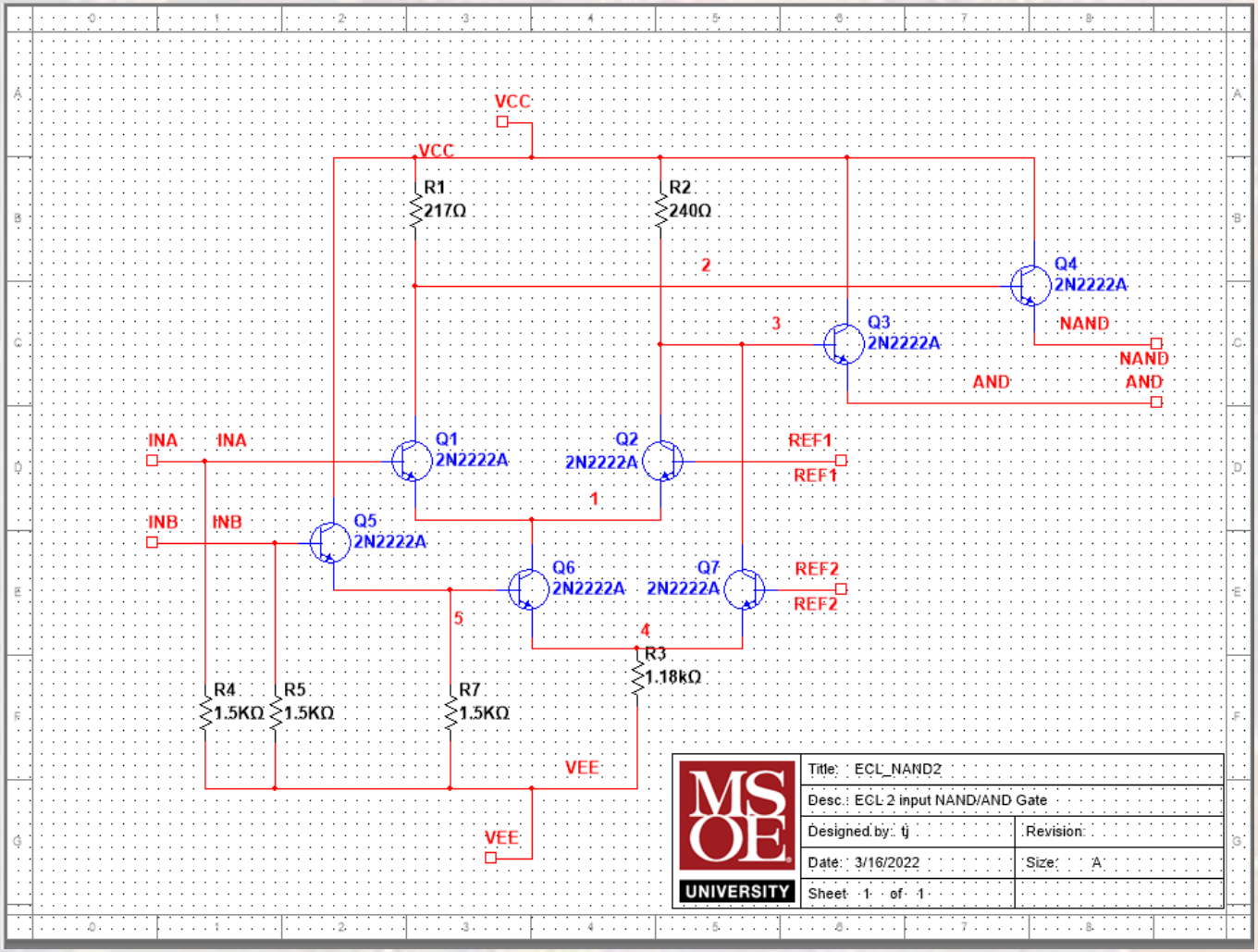
Emitter Coupled Logic - Implementation

- 3 Input NOR/OR



Emitter Coupled Logic - Implementation

- 2 Input NAND/AND



Emitter Coupled Logic - Implementation

- Reference Generator - 2