

- 1 – Analyze and draw V_{R2} vs V_{batt} for circuit 1 with V_{batt} ramping from 0V to 5V (assume $V_D = 0.7V$, be sure to indicate V_{batt} voltages of interest) 20pts

- 2 – Create a truth table for circuit 2 and indicate the output voltage for each state (assume the inputs are 0 and 3.3V and $V_D = 0.7V$) 20pts

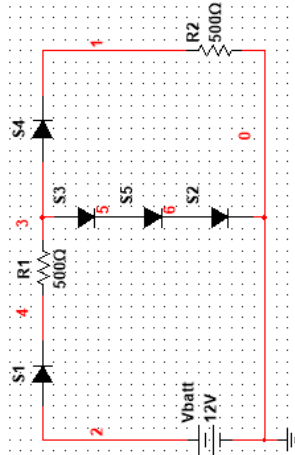
- 3 – Determine the voltages $V(3)$ and $V(6)$ in circuit 3 for input voltages (V_{in}) of 0.5V, 1.5V, 2.5V, 3.5V and 4.5V. Assume $V_{BEon} = 0.65V$ for both transistors and $\beta_{npn} = 200$, $\beta_{pnp} = 185$. 20pts


4 – Simulate circuit 3 and provide the simulated values for $V(3)$ and $V(6)$. Provide a plot or DC analysis points. 30pts

5 – Explain any discrepancies:

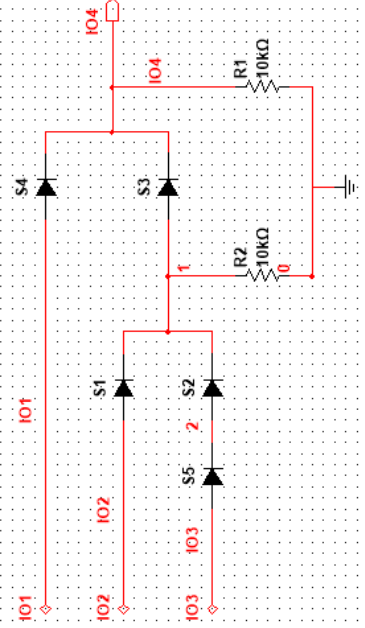
10 pts


Circuit 1 - circuit for prob 1



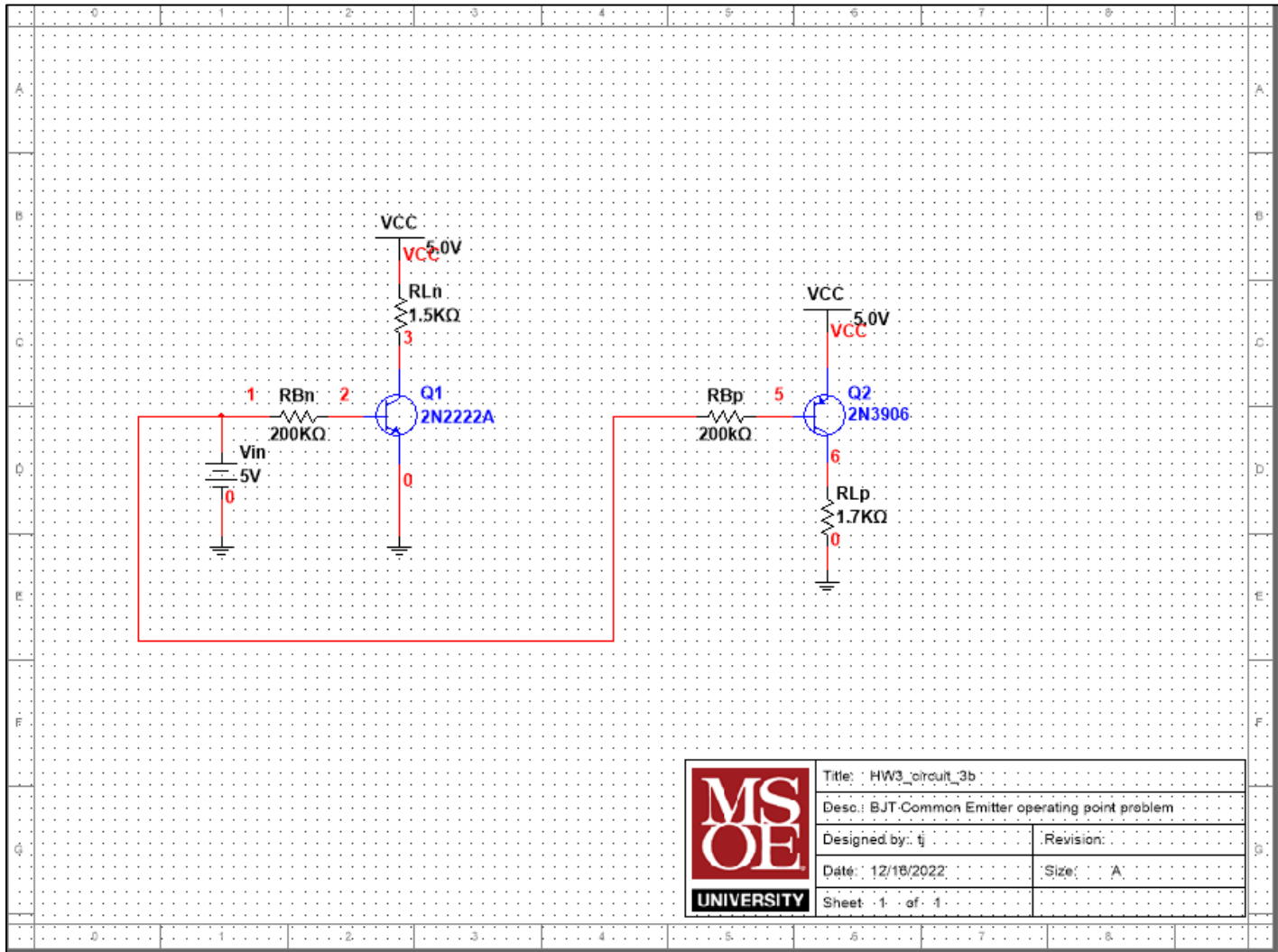
		Title: HW3_circuit_1b
		Desc: HW3 - Circuit 1 - hand analysis
Designed by: tj		Revision:
Date: 12/10/2022		Size: A
Sheet 1 of 1		


Circuit 2 - circuit for prob 2



		Title: HW3_circuit_2b
		Desc: HW3 - Circuit 2 - hand analysis
Designed by: tj		Revision:
Date: 12/10/2022		Size: A
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Circuit 3 - circuit for probs 3, 4, 5



	Title: HW3_circuit_3b	
	Desc: BJT-Common Emitter operating point problem	
	Designed by: tj	Revision:
	Date: 12/18/2022	Size: A
	Sheet: 1 of 1	