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1 – Simulation: Compare the basic TTL NAND gate (TTL basics – slide 7) delay to the Enhanced Totem-Pole TTL Nand (TTL Basics – slide 9) gate delay. Assume 0.8v – 3v inputs, 5V VCC, and a 20KΩ || 15pF load. Provide schematics, transient plots and delay comparisons. 40pts

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2 – Simulation: Compare the Enhanced Totem-Pole TTL Nand gate (TTL Implementation – slide 3) delay to the Schottky modified version (TTL Implementation – slide 5). Assume 0.8v – 3v inputs, 5V VCC, and a 20KΩ || 15pF load. Provide schematics, transient plots and delay comparisons. 40pts

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3 – Simulation / Design Comprehension: One component in the Enhanced Totem-Pole TTL Nand gate can be modified to reduce the rise time. Think through which component would have the largest impact and simulate the rise time for 3 values of the component (use sufficient values to see approx. 50% improvement). Same inputs as #1 and #2. Provide plots and delay comparisons. 20pts