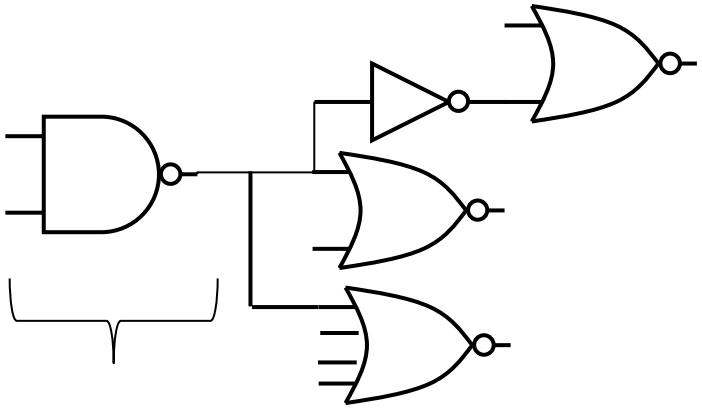
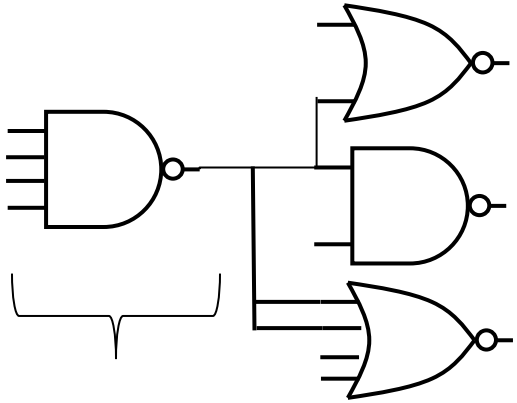
CE 3101 HW6 Name_____

1 – Analysis: Given the gate information below, calculate the t_{pd} for the indicated nand gate 30pts

Gate	INV	2-NAND	2-NOR	4-NAND	4-NOR
Input load factor (LE)	0.8	1.0	2.0	1.66	3.33
Fixed delay factor	25ps	35ps	35ps	50ps	50ps
Variable delay factor	15ps/LE	20ps/LE	20ps/LE	30ps/LE	30ps/LE





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2 – Research: Using the spec sheet for the 74HCT04 part on the Lab webpage, determine the maximum number of loading inverters that can be tied to a single driving inverter and ensure the specified delay will not be violated

Propose a solution to drive a 150pF load while maintaining the specified gate delay 40pts

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3 – Analysis: Estimate the gate delay for the following inverter 30pts

$k'_n = 15uA/V^2$	$V_{tn} = 0.6V$	Wn = 10um, Ln = 2um	$Cgn = 20fF/u^2$
$k'_p = 5uA/V^2$	$V_{tp} = -0.6V$	Wp = 30um, Lp = 2um	$Cgp = 22fF/u^2$
Vdd = 1.8V			

a) Driving a 5pF load

b) Driving 5 identical inverters