CE3101 Lab 4: Bipolar Logic Circuits

Objectives

- Explore ECL and TTL circuits

Prelab **student check off**

- Checkout an Analog Discovery 2 kit from the Tech Center ☐
- Checkout needed components from the Tech Center
- ☐

***** these circuits are using +5V, and Gnd for the supplies *****

Assignment

Part 1: Simulation: Create a 2 input ECL NOR gate schematic as a hierarchical block. Create a lab4_part1 schematic that places 4 of these NOR gates in it. Connect the 1st NOR gate to a voltage pulse source. Daisy-chain the nor output of each gate to one input of the next. Tie the unused inputs to 3.5V.

a) Set the voltage pulse source to 3.5v-4.5v, 1ms delay, width, rise, fall times and 4ms period. Measure the switching point (rising/falling) of NOR gate 3 (input vs output)

b) Set the voltage pulse source to 3.5v-4.5v, 1us delay, 1us width, 1ns rise and fall times and 2us period. Measure tr, tf and the gate delay of NOR gate 3 (input switching point to output switching point from part a) ☐

Part 2: Simulation: Create a 2 input TTL NAND gate schematic as a hierarchical block. Create a lab4_part2 schematic that places 4 of these NAND gates in it. Connect the 1st NAND gate to a voltage pulse source. Daisy-chain the output of each gate to one input of the next. Tie the unused inputs to 3.9V.

a) Set the voltage pulse source to 0v-3.9v, 1ms delay, width, rise, fall times and 4ms period. Measure the switching point (rising/falling) of NAND gate 3 (input vs output)

b) Set the voltage pulse source to 0v-3.9v, 1us delay, 1us width, 1ns rise and fall times and 2us period. Measure tr, tf and the gate delay of NAND gate 3 (input switching point to output switching point from part a) ☐

Part 3: Implementation:

a) Get a 74LS00N quad NAND gate part from the tech center. Wire it up just like part 2. Use the Analog discovery to measure the switching points, tr, tf and gate delays. ☐

Check Off

- Demo and document part 1 30%
- Demo and document part 2 30%
- Demo and document part 3 40%

Demo (in-person or via Teams chat) and Report (in the box) due by 4:00 pm Wednesday of the week following the lab.