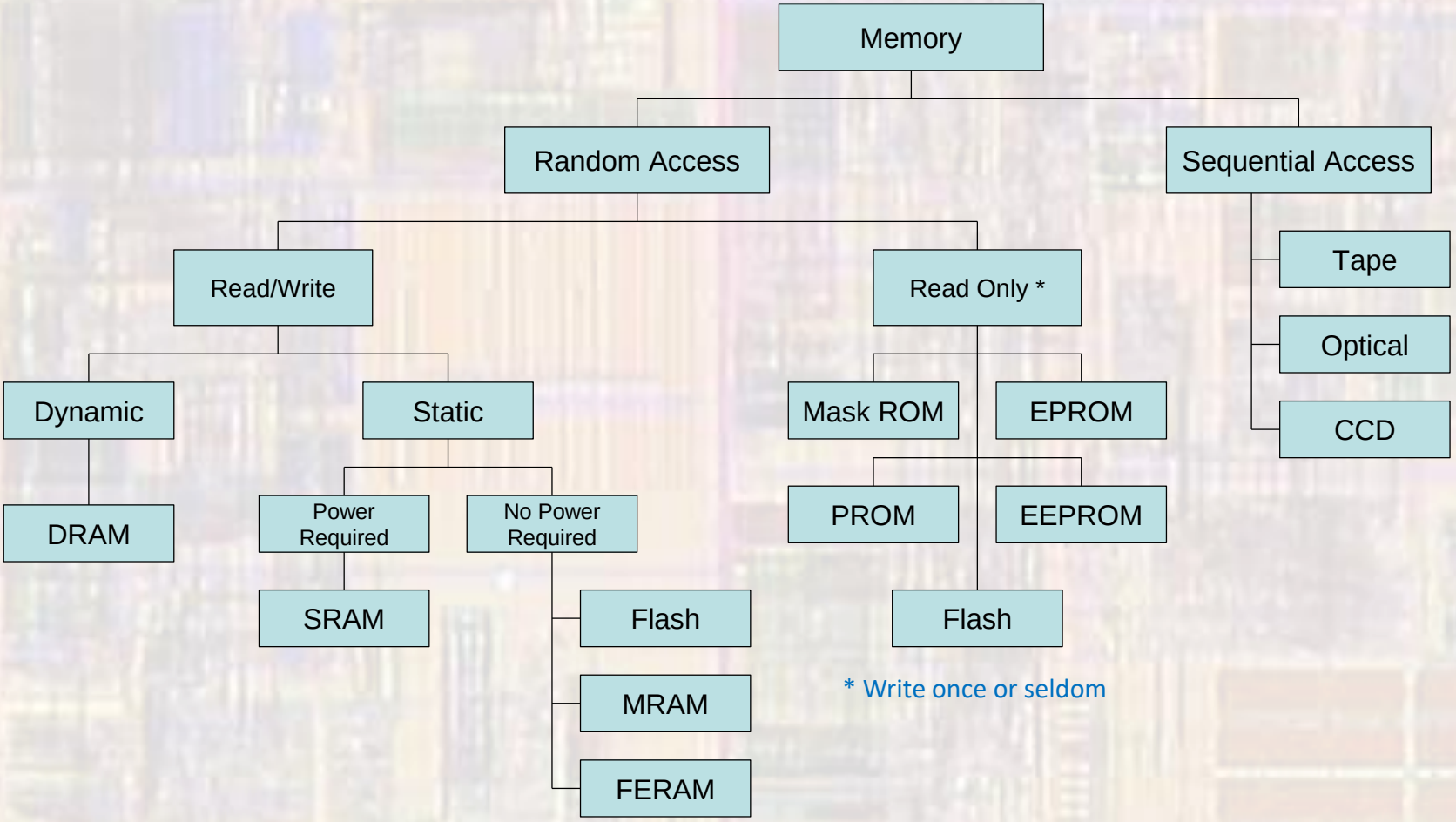
SDRAM

Last updated 4/28/22

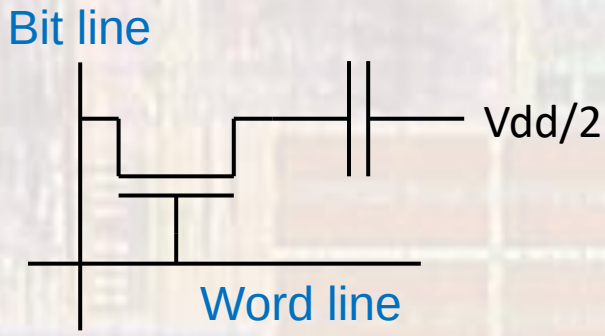
Memory - SDRAM

- Memory Taxonomy



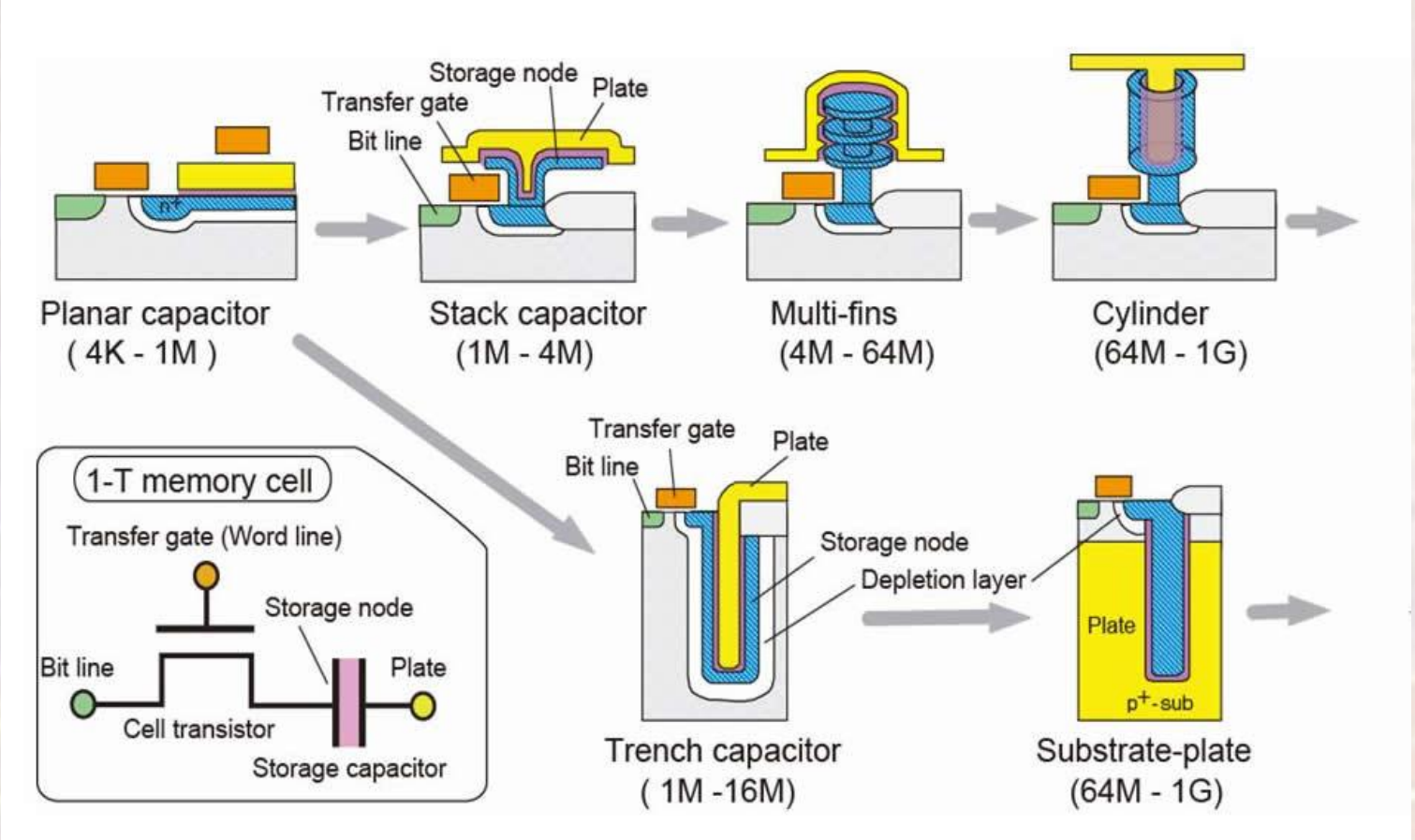
Memory - SDRAM

- SDRAM – Synchronous Dynamic Random Access Memory
  - Memory cell (1 bit) is based on capacitor charge storage
  - Bit value decays over time
    - must be recharged – called a refresh cycle
  - Standard SDRAM transfers 1 word each array access
    - DDR – double data rate – transfers 2 words each array access
    - DDR2, DDR3, DDR4 – transfer 4,8,16 words each array access
  - Medium speed
  - Highest density
  - Used as main memory



Memory - SDRAM

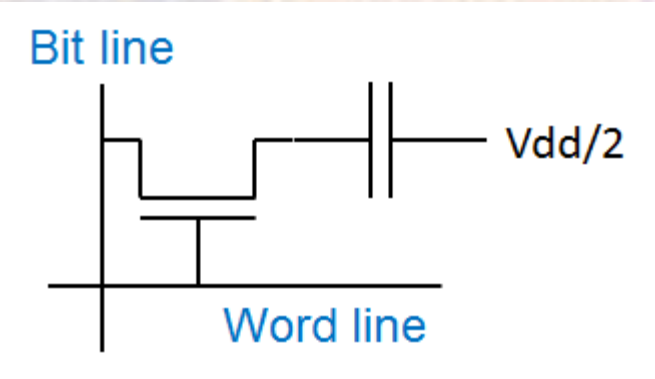
- SDRAM – Cell

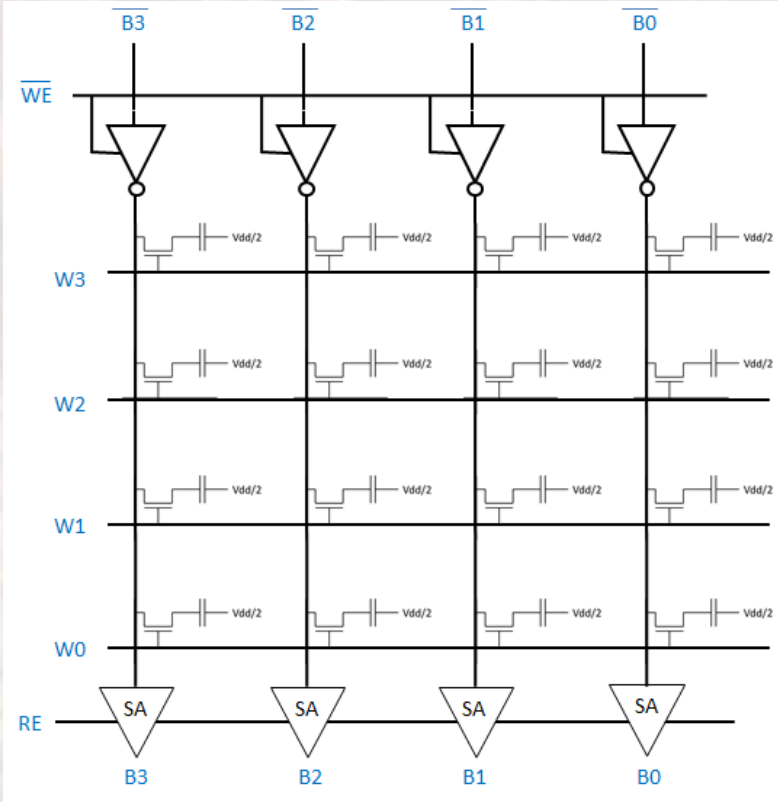


Src: IEDM

Memory - SDRAM

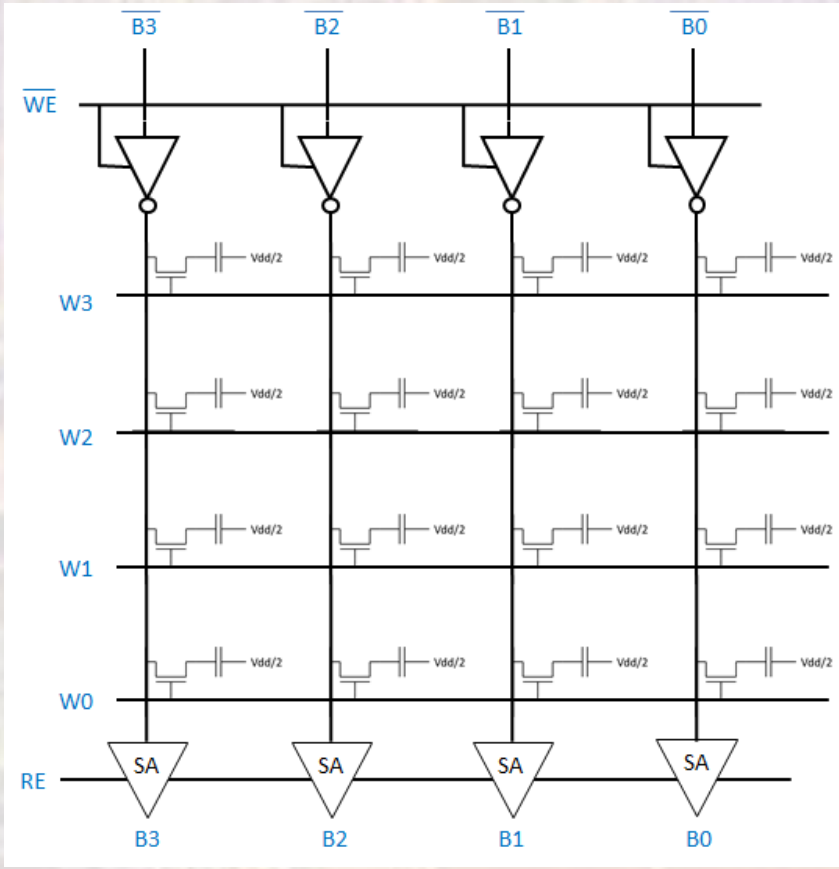
- SDRAM – Synchronous Dynamic Random Access Memory
  - Write
    - All Word lines low
    - Read Enable (RE) disabled (low)
    - Place $\overline{B0}$, $\overline{B1}$, $\overline{B2}$, $\overline{B3}$ on inputs
    - Pull write enable bar ($\overline{WE}$) low
    - Strobe the desired word line high
    - Bit lines write to the bit cell capacitors





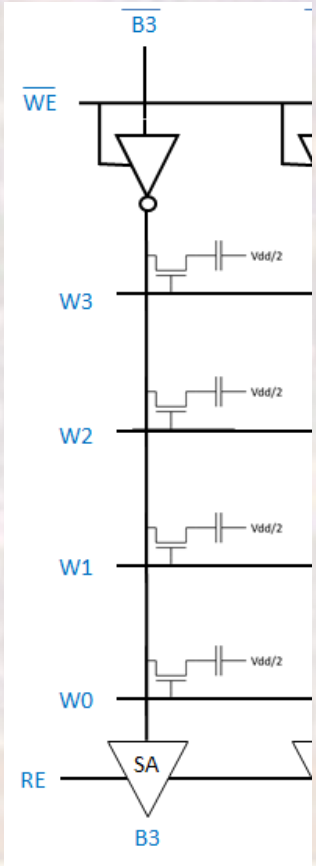
Memory - SDRAM

- SDRAM – Synchronous Dynamic Random Access Memory
  - Read
    - All Word lines low
    - Write enable bar ($\overline{WE}$) high
      - inverters tristated
    - Read Enable (RE) high
    - Strobe the desired word line high
    - Sense amplifiers read the value of the capacitors
    - The read process is destructive !
      - WHY?



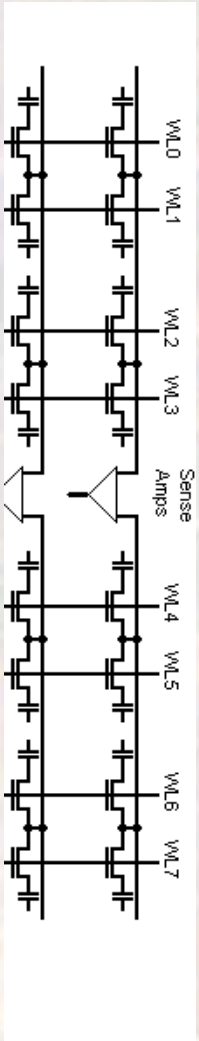
Memory - SDRAM

- SDRAM – Dynamics
  - C_{cell} ~ 1/10 $C_{bitline}$
  - Charge redistribution → small voltage changes
  - Cell charge = Q_{cell} = +/- (Vdd/2 * C_{cell})
  - Bitline charge = $Q_{bitline}$ = Vdd/2 * $C_{bitline}$
    - Assuming $V_{bitline}$ precharged to Vdd/2
  - $\Delta V = \frac{V_{dd}}{2} \times \left(\frac{C_{cell}}{C_{cell}+C_{bitline}}\right) = 0.045V_{dd} = 122\text{mV} \text{ @ } 2.7\text{V}$



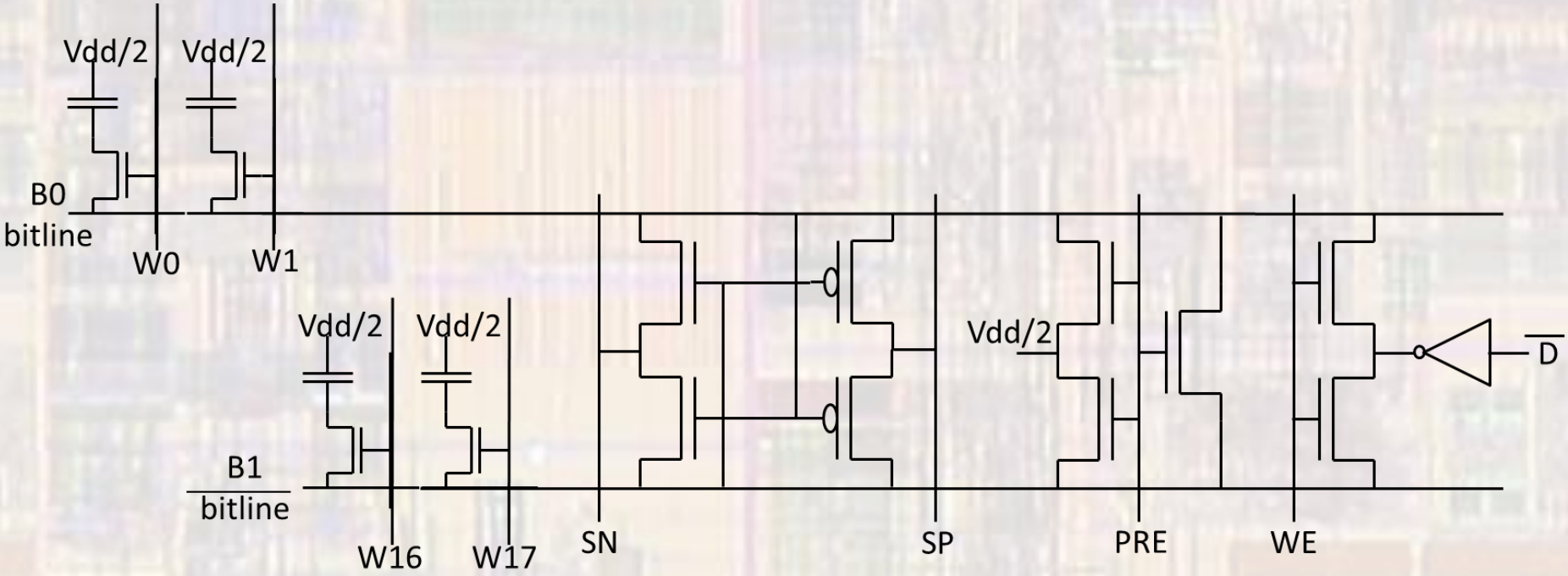
Memory - SDRAM

- SDRAM – Dynamics
  - Use a differential amplifier for sensing
    - But what is the second input?
      - Break the array into pieces
      - Precharge all bitlines
      - Compare a bitline from selected wordline to one from a non-selected wordline
  - Open Bitline array
    - Control the signal swing by size of bitline segments
    - Compare precharged non-word selected bitlines with small swing word selected bitlines
  - Alternate configurations include folded and twisted
    - Less dense but offer better noise characteristics
    - Trade off size of segments for # of sense amps



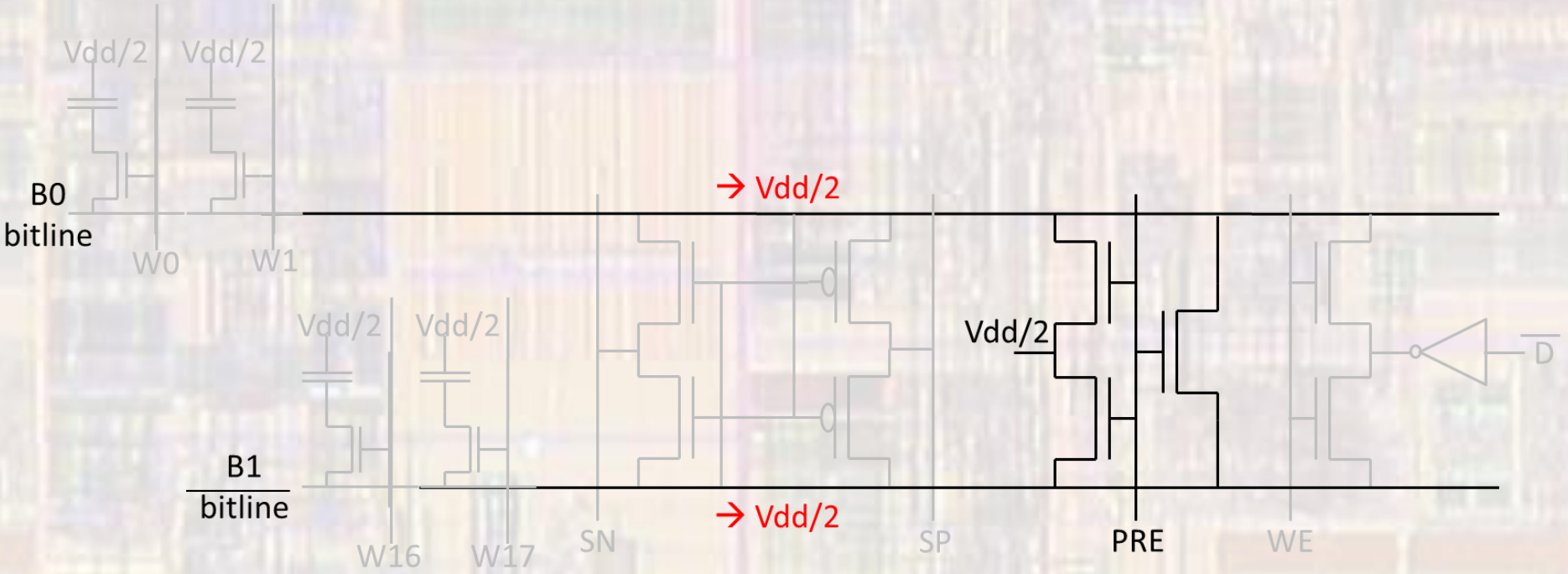
Memory - SDRAM

- SDRAM – Sense amplifier



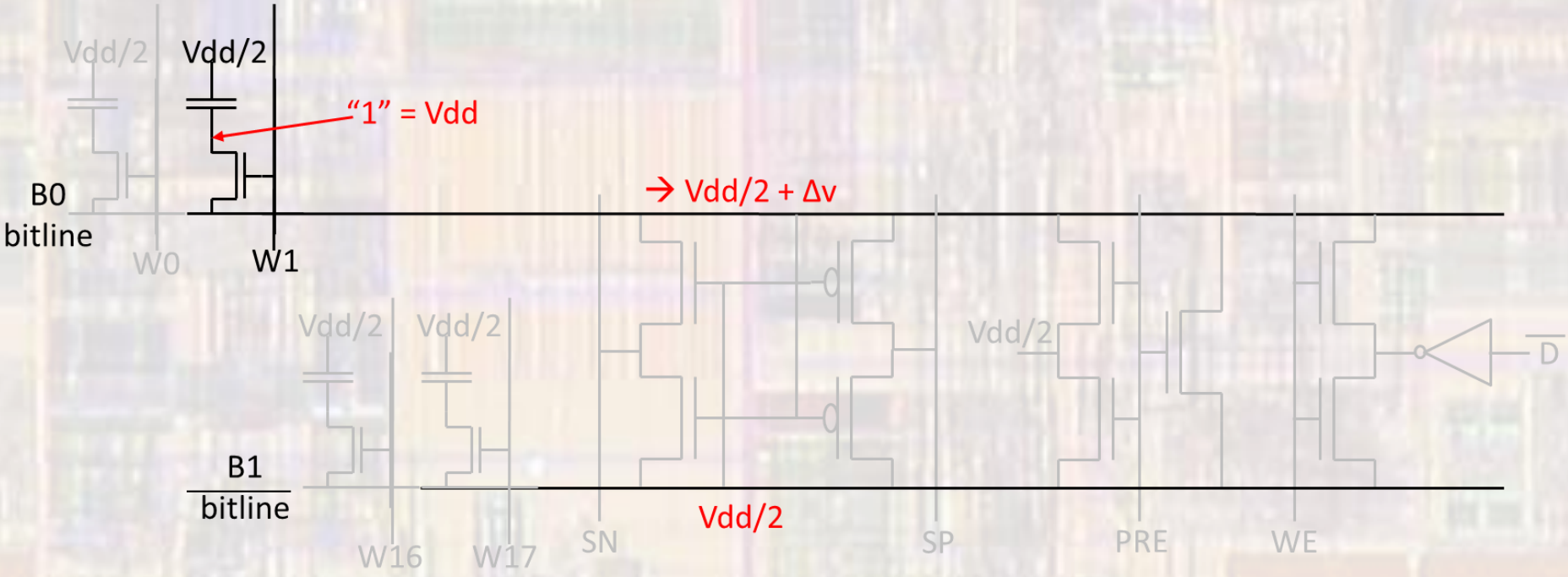
Memory - SDRAM

- SDRAM – Sense amplifier
  - Phase 0 - PRECHARGE



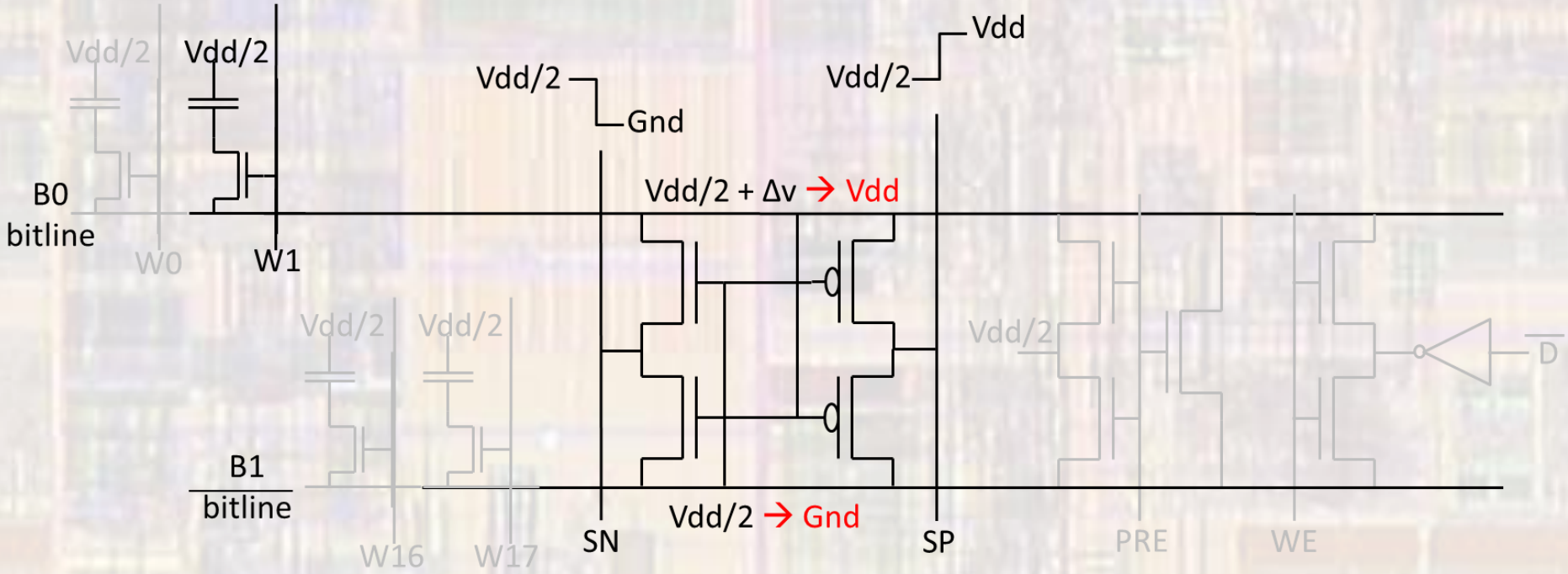
Memory - SDRAM

- SDRAM – Sense amplifier
  - Phase 1 - ACCESS



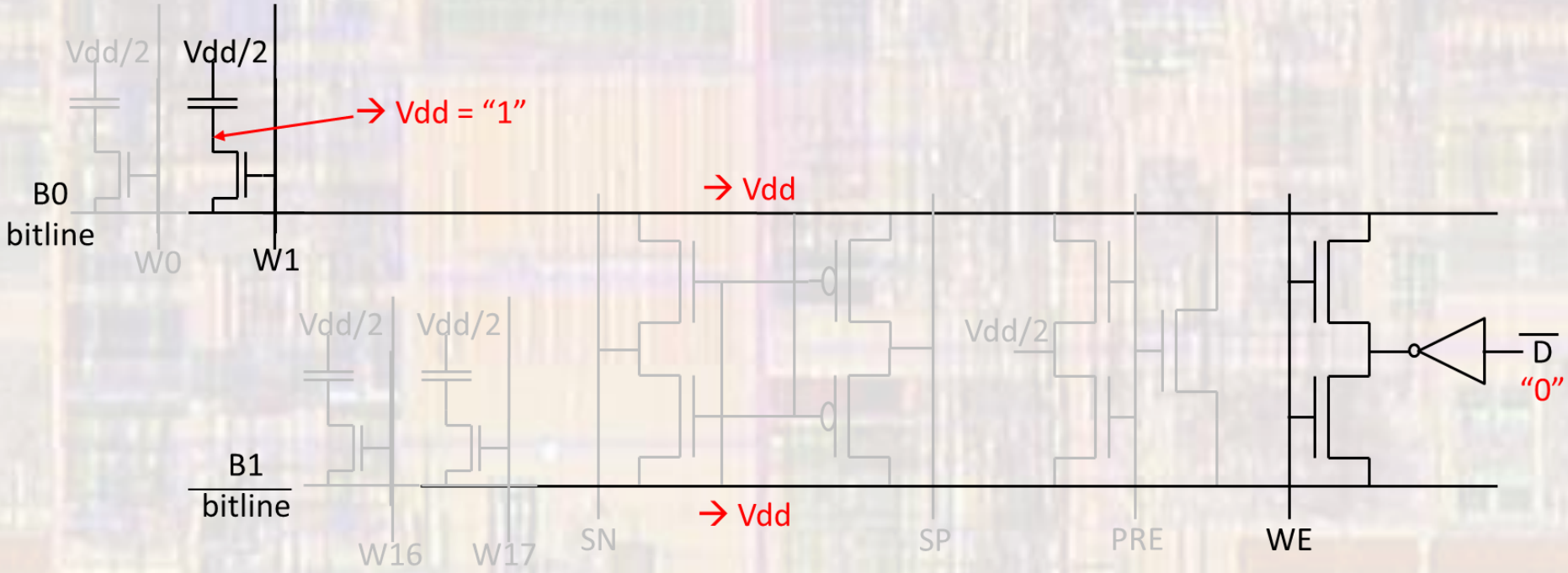
Memory - SDRAM

- SDRAM – Sense amplifier
  - Phase 2 – SENSE (and Restore)



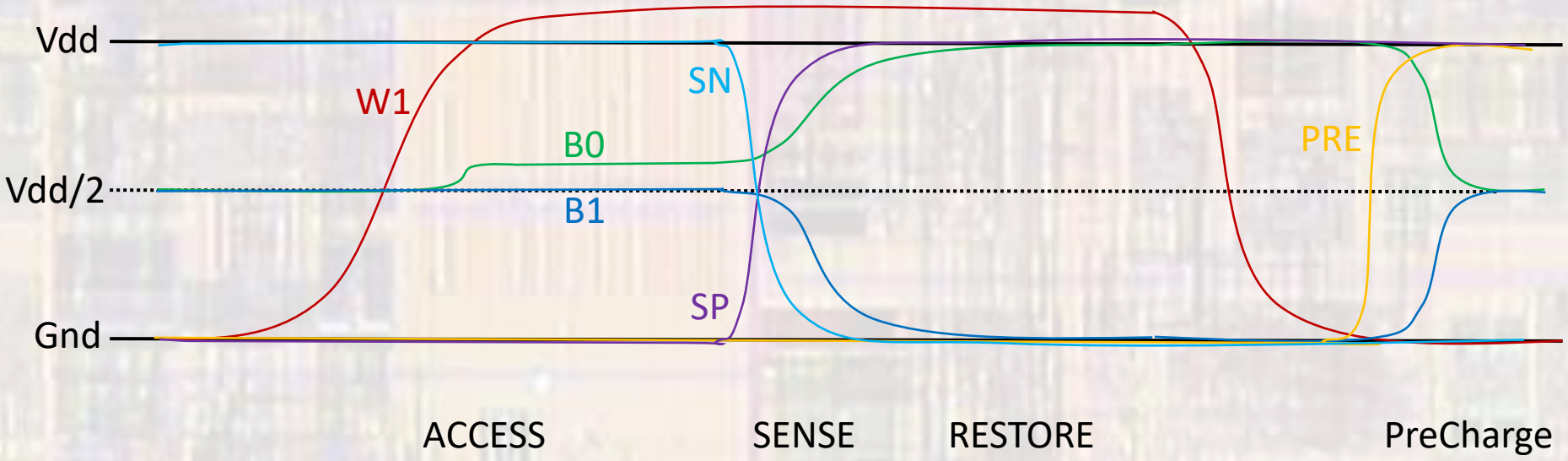
Memory - SDRAM

- SDRAM – Sense amplifier
  - WRITE



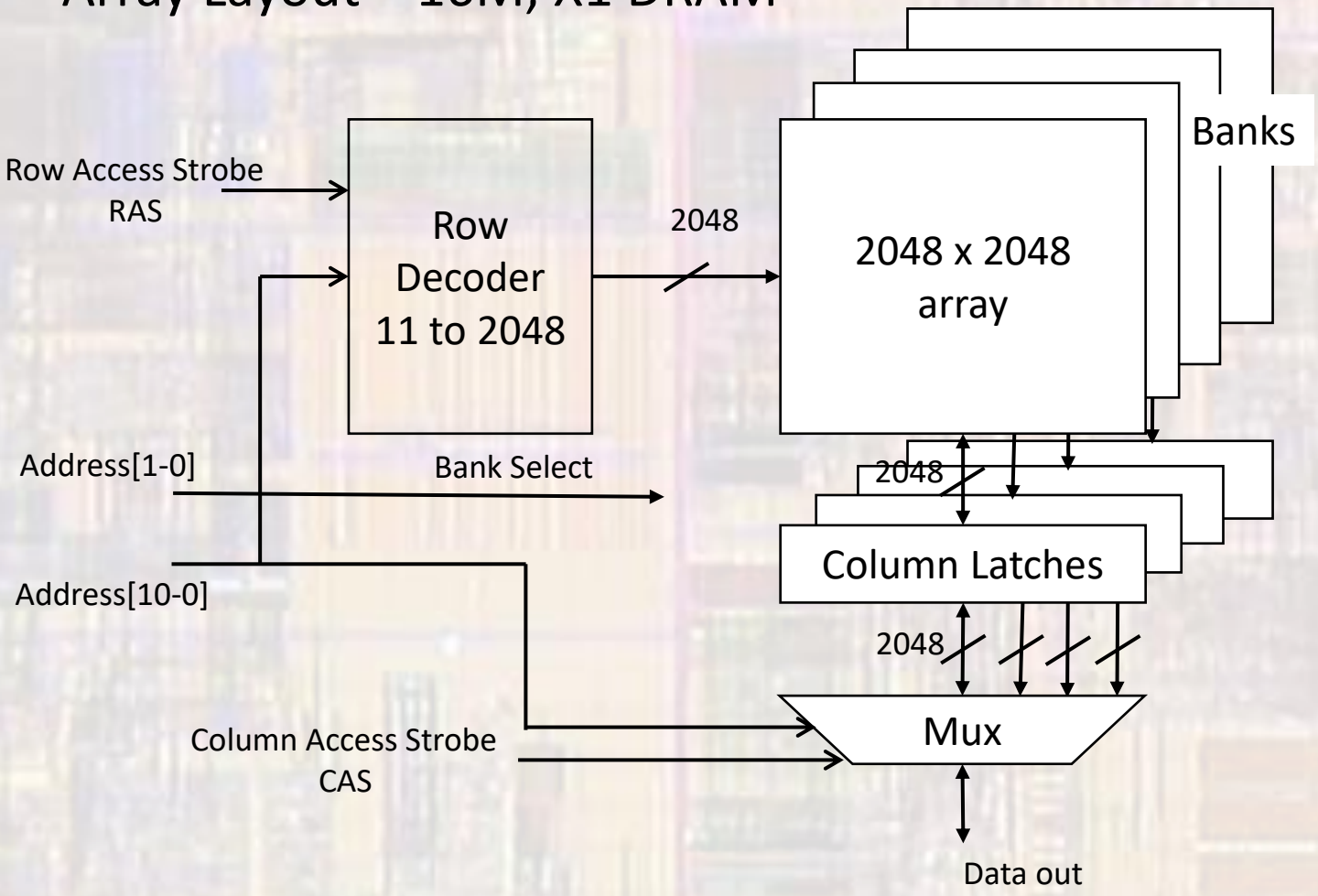
Memory - SDRAM

- SDRAM – Sense amplifier



Memory - SDRAM

- SDRAM - Banks
  - Array Layout – 16M, X1 DRAM



Memory - SDRAM

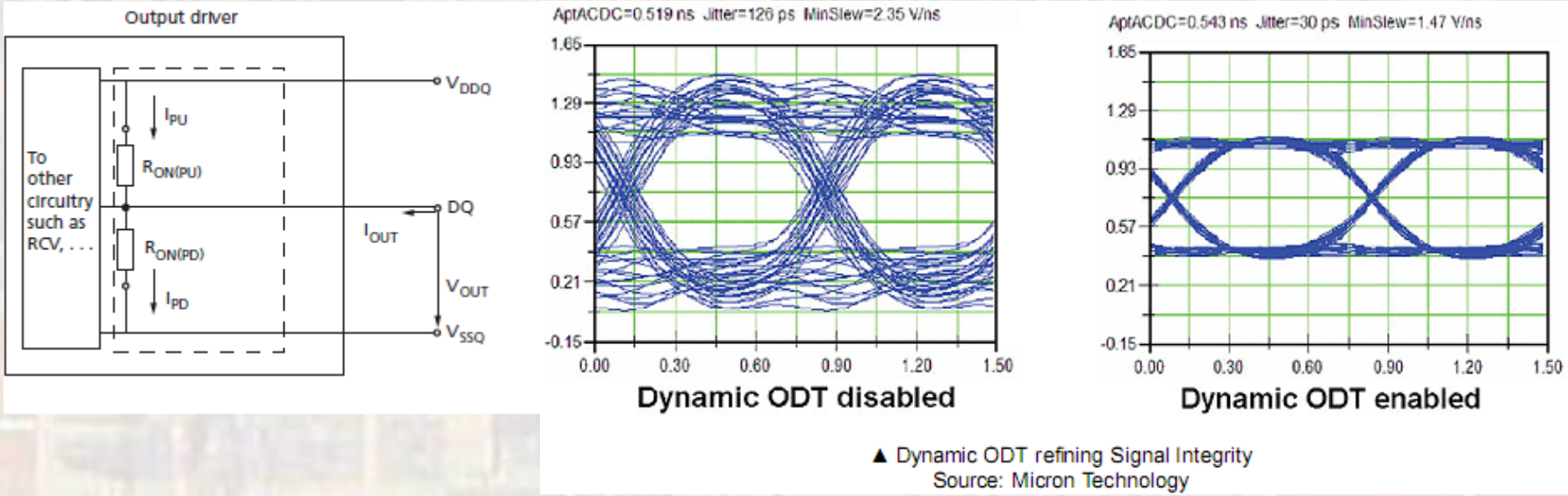
- SDRAM – Pipelining
  - Allow next read/write process to start while current r/w is in process
  - With proper timing you can achieve 100% throughput on
    - Access to a new column on an open row
    - Opening a new row on an alternate bank
  - More to come

Memory - SDRAM

- SDRAM – Strobe Based Data Bus
  - Very high operating speeds lead to concerns about
    - Trace lengths, transmission line effects, clock skew, …
  - Add a strobe signal for every output beat (DQS)
  - On reads
    - Strobe is generated by the SDRAM edge aligned with the data
    - MMU offsets the strobe by 90 degrees and uses it to capture the data
  - On writes
    - Strobe is generated by the MMU and offset by 90 degrees wrt data
    - SDRAM uses the strobe to capture the write data
  - Strobes include a preamble, postamble and write leveling

Memory - SDRAM

- SDRAM – On Die Termination (ODT)
  - Very high operating speeds lead to concerns about
    - Trace lengths, transmission line effects, clock skew, …
  - Place programmable resistors on die to terminate the transmission lines for critical signals, DQ, DQS, CLK



▲ Dynamic ODT refining Signal Integrity
Source: Micron Technology

Memory - SDRAM

- SDRAM – Read/Write Leveling
  - Write and Read Leveling is to allow some mechanism for the memory controller to adjust internal DQS to compensate for unbalanced loading on the board for write and read operation

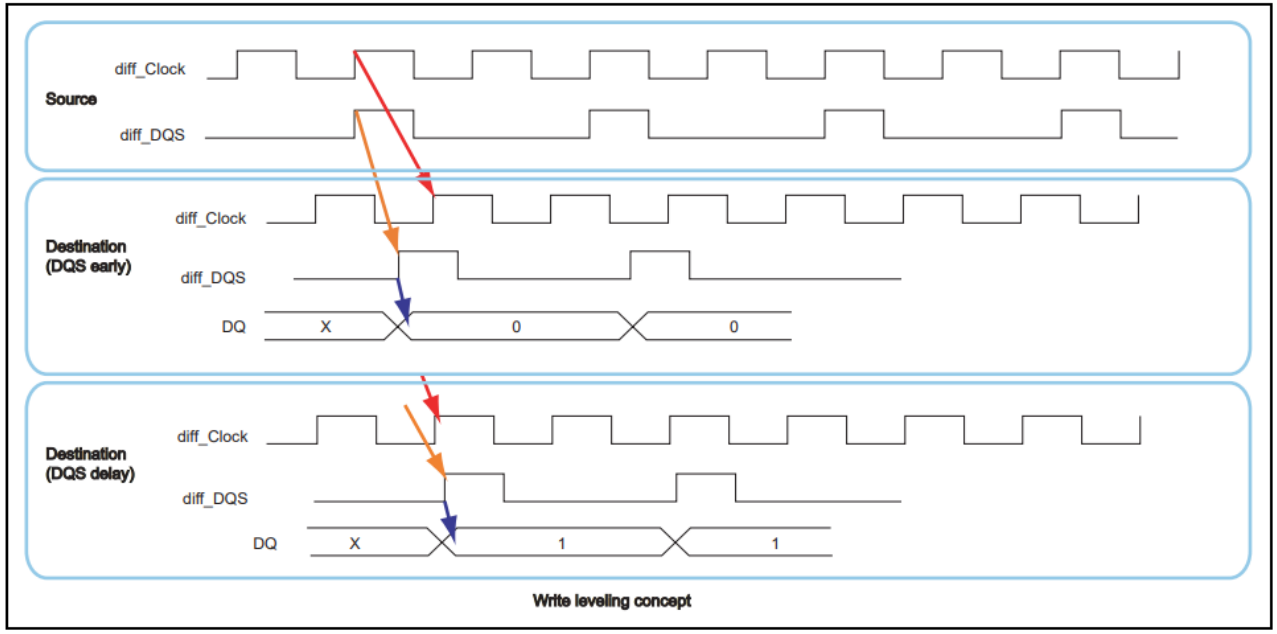


Figure 1-7 Conceptual Diagram of Write Leveling

