SDRAM Operation

Last updated 4/28/22

SDRAM - Operation

- SDRAM
  - 512Mb : 128Mx4, 64Mx8, 32Mx16

The 512Mb SDRAM is a high-speed CMOS, dynamic random-access memory containing 536,870,912 bits. It is internally configured as a quad-bank DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the x4's 134,217,728-bit banks is organized as 8192 rows by 4096 columns by 4 bits. Each of the x8's 134,217,728-bit banks is organized as 8192 rows by 2048 columns by 8 bits. Each of the x16's 134,217,728-bit banks is organized as 8192 rows by 1024 columns by 16 bits.

Read and write accesses to the SDRAM are burst-oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA[1:0] select the bank; A[12:0] select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

SDRAM - Operation

- SDRAM
  - 512Mb : 128Mx4

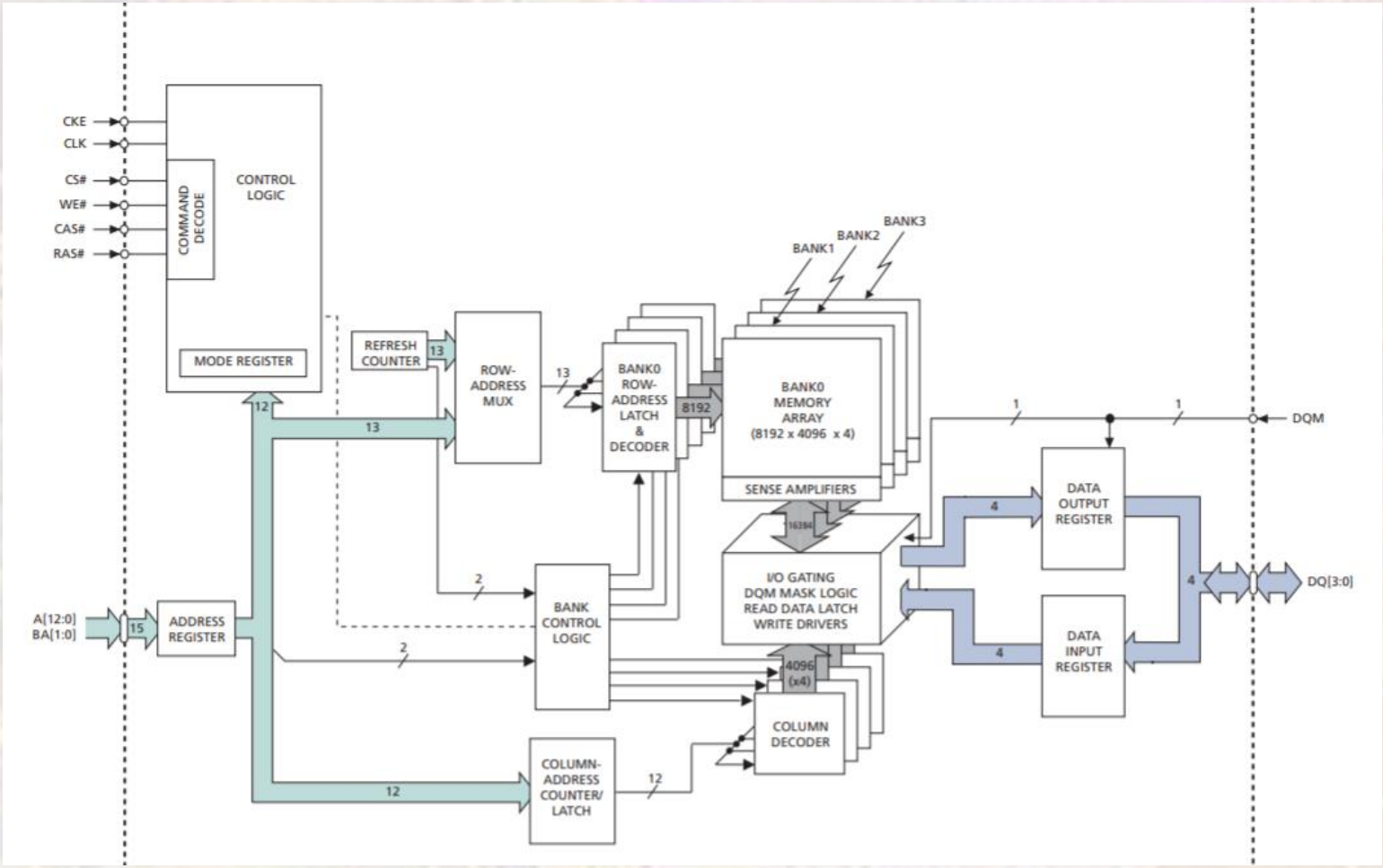
The SDRAM provides for programmable read or write burst lengths (BL) of 1, 2, 4, or 8 locations, or the full page, with a burst terminate option. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

The 512Mb SDRAM uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2n rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a highspeed, fully random access. Precharging one bank while accessing one of the other three banks will hide the PRECHARGE cycles and provide seamless, high-speed, random-access operation.

SDRAMs offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks to hide precharge time, and the capability to randomly change column addresses on each clock cycle during a burst access.

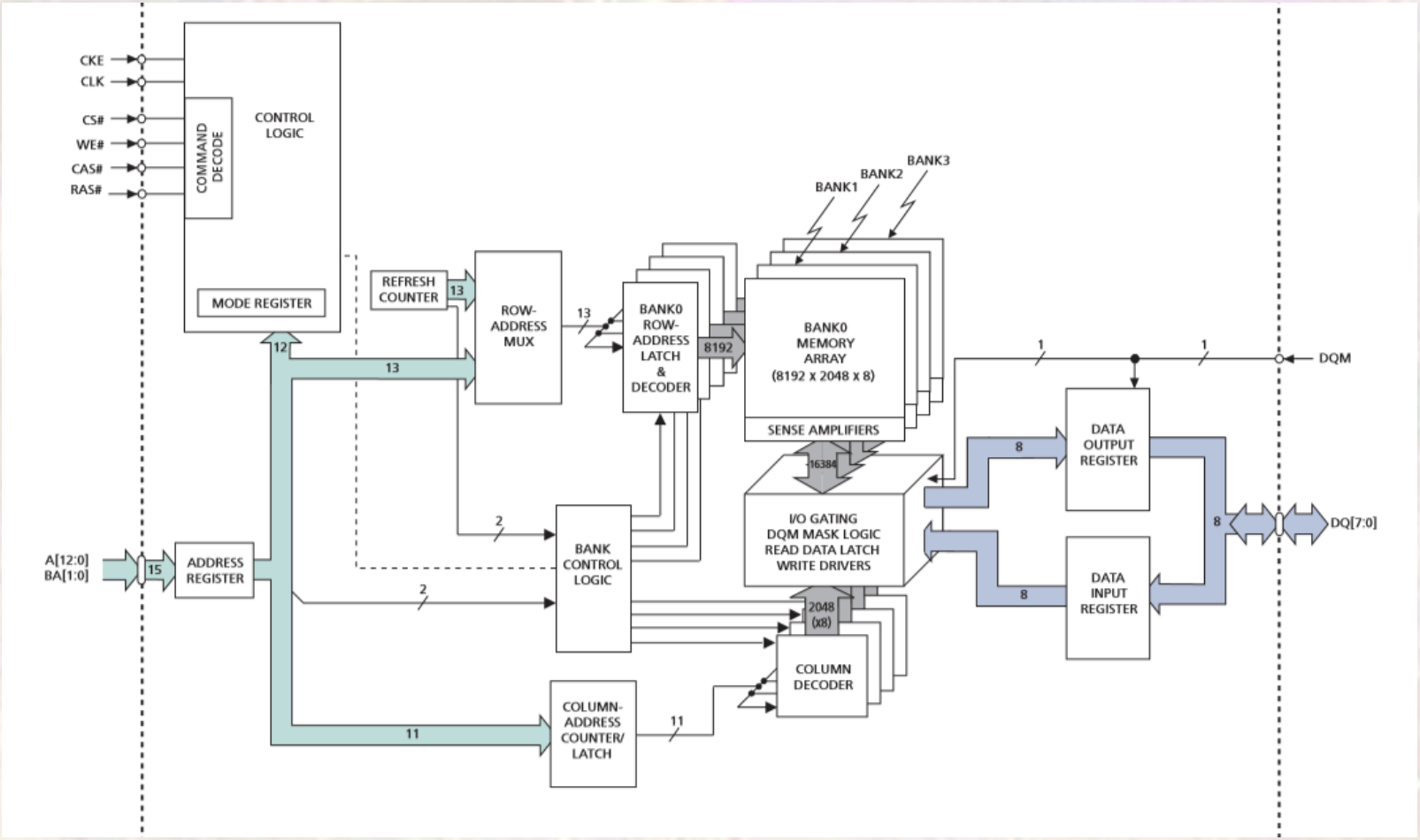
SDRAM - Operation

- SDRAM
  - 512Mb : 128Mx4



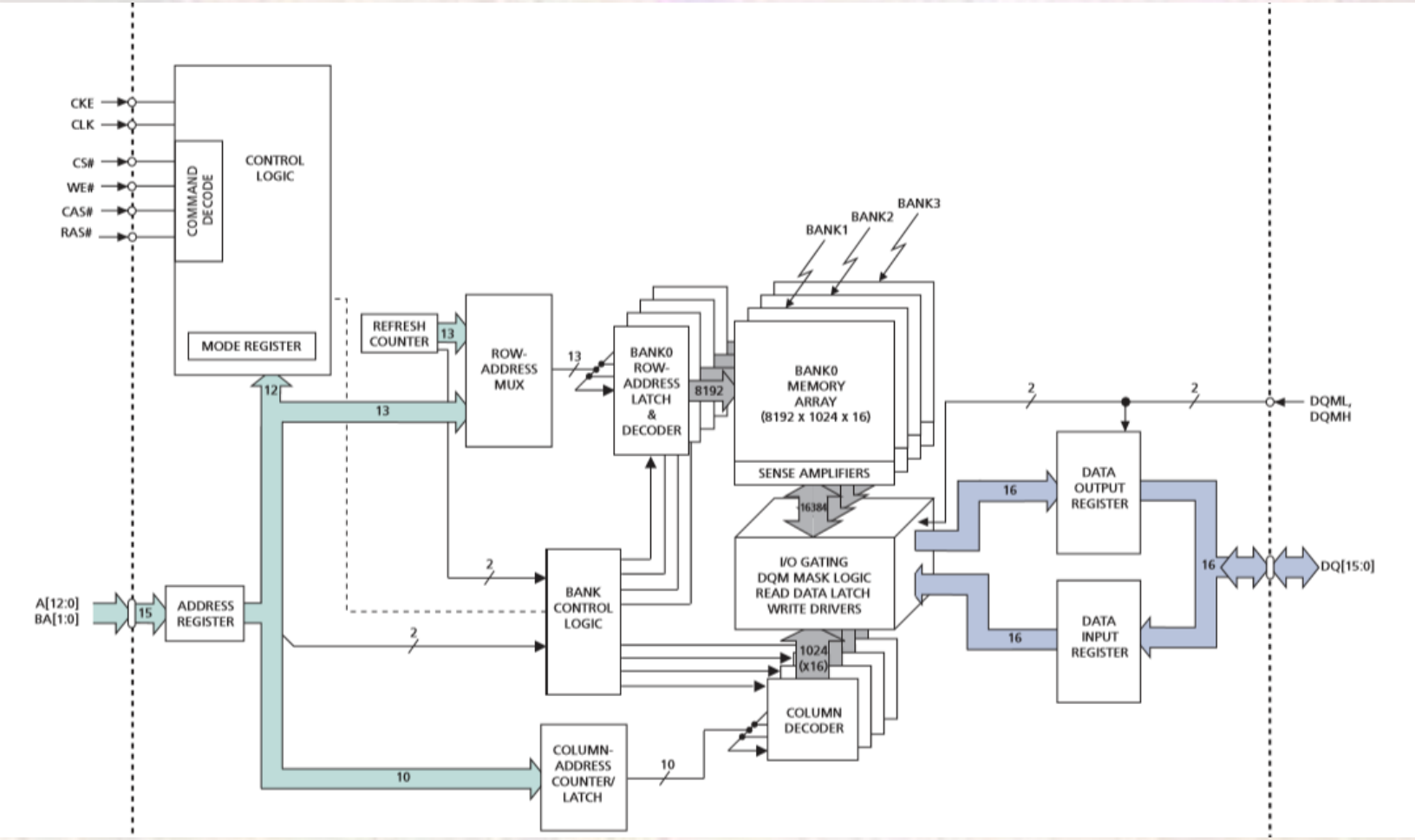
SDRAM - Operation

- SDRAM
  - 512Mb : 64Mx8



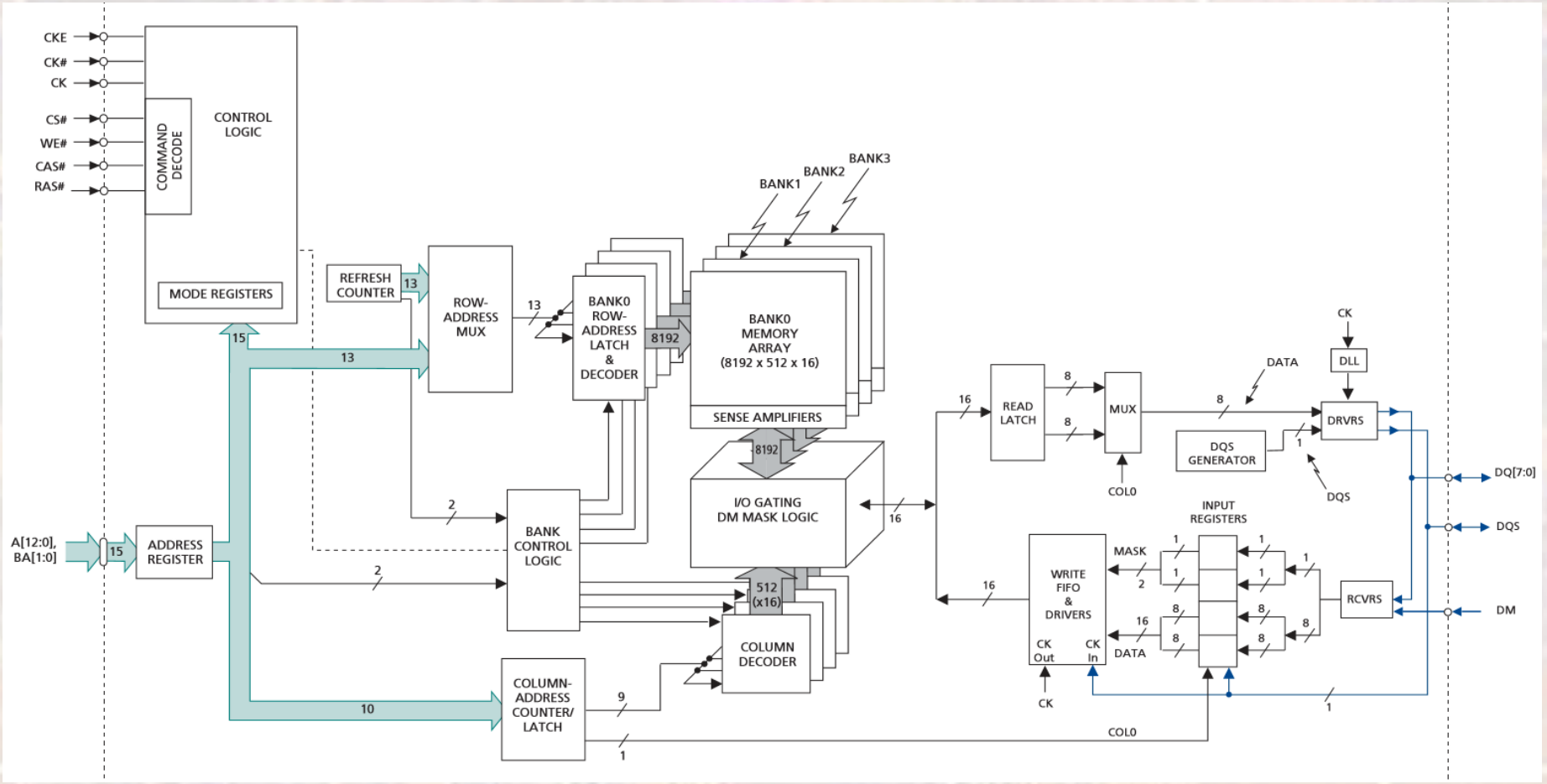
SDRAM - Operation

- SDRAM
  - 512Mb : 32Mx16



SDRAM - Operation

- SDRAM – DDR
  - 256Mb : 32M x 8

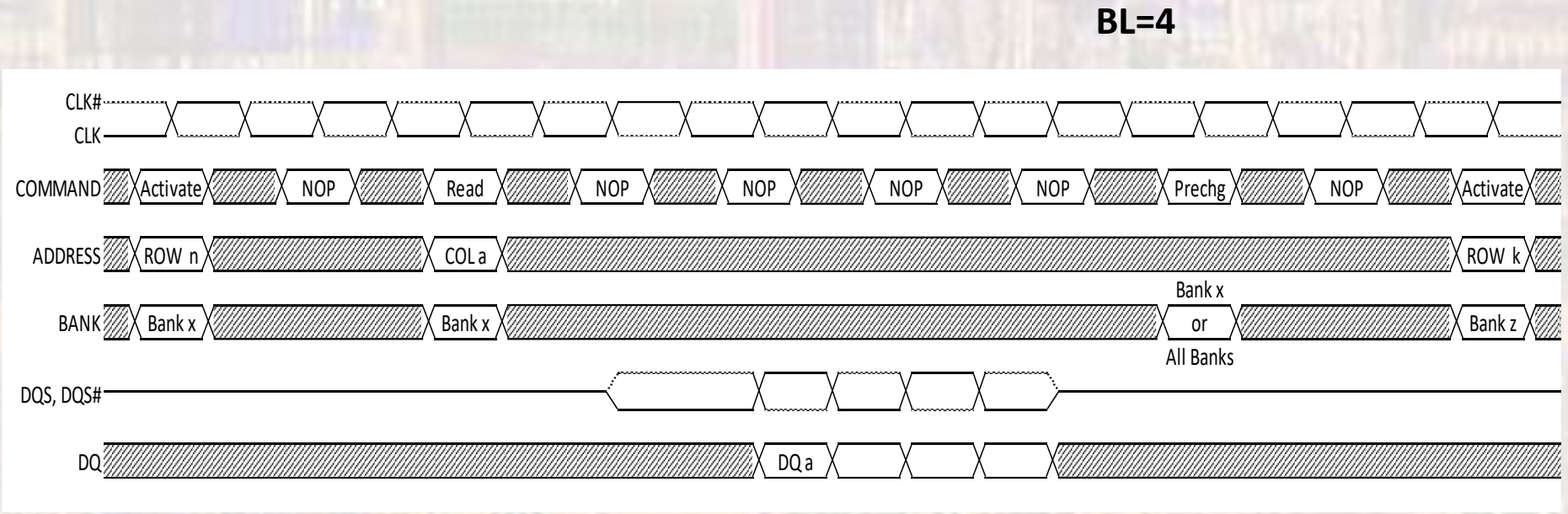


SDRAM - Operation

- SDRAM – Basic Commands
  - ACTIVATE – select 1 row in a specific bank (RAS) (open)
  - READ/WRITE – select a column (CAS)
  - PRECHARGE – prepare 1 or all banks for activation (close)
    - Auto precharge – automatically executes precharge after a Read or Write
  - NOP – do nothing
  - Commands are decoded from the CS, RAS, CAS, and WE signals

SDRAM - Operation

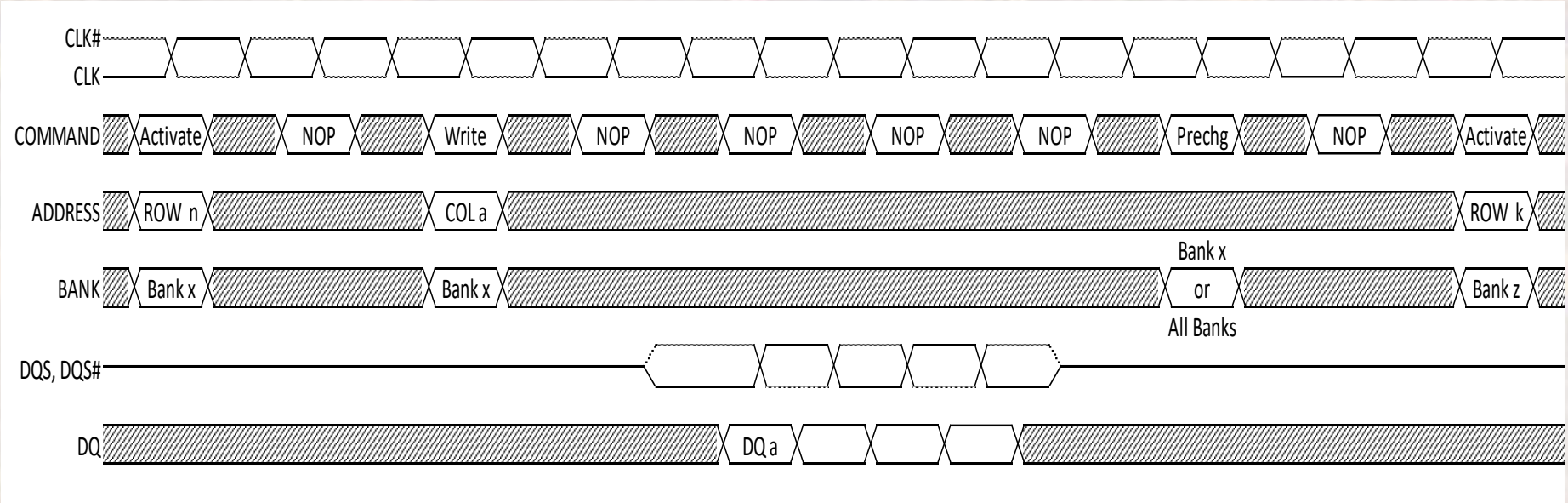
- SDRAM – Timing
  - Read



SDRAM - Operation

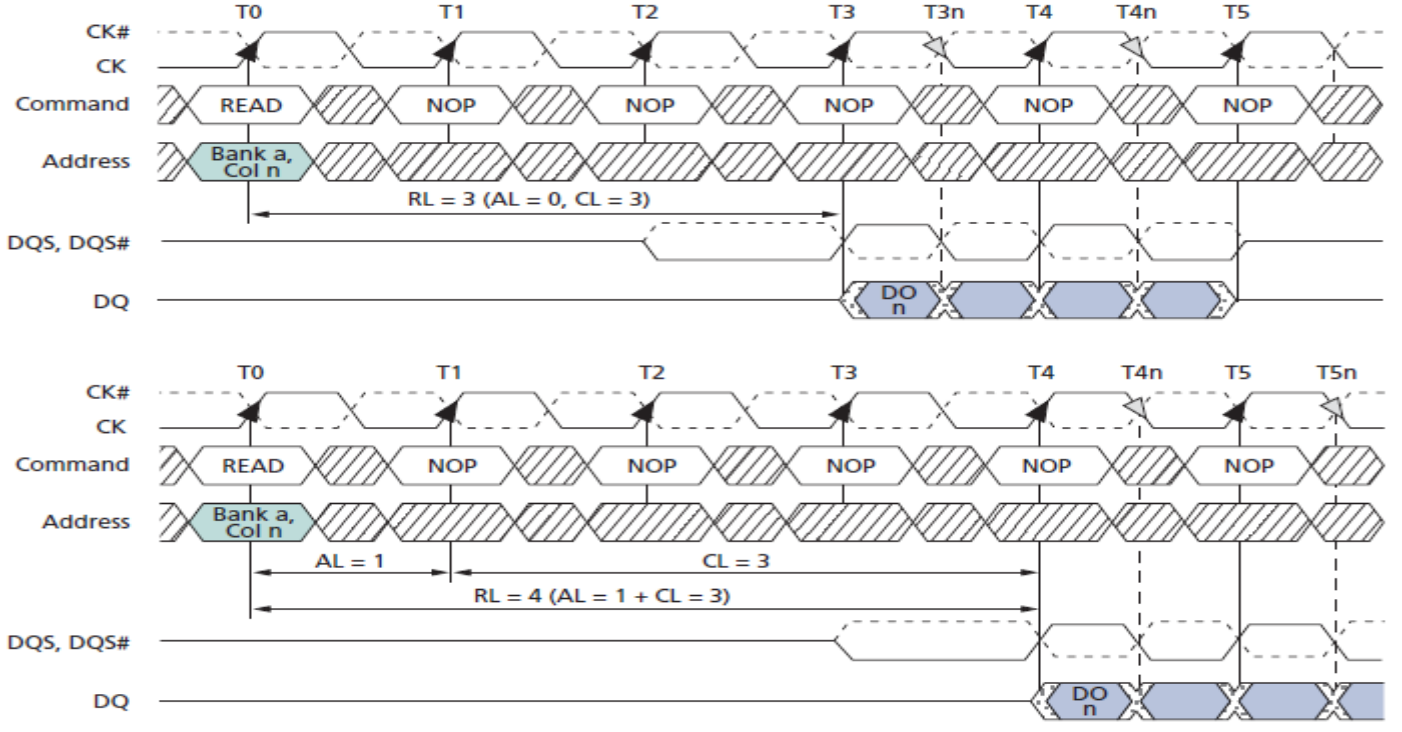
- SDRAM – Timing
  - Write

BL=4



SDRAM - Operation

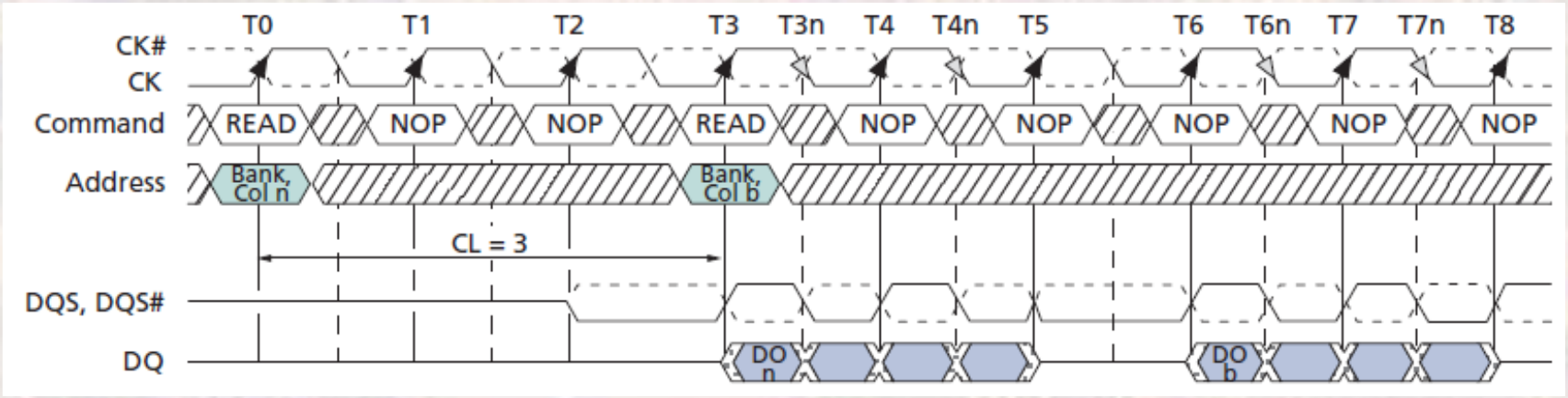
- SDRAM – Timing
  - Read Latency
    - CL – CAS latency – clock cycles from CAS to data out
    - AL – Additional Latency – pipeline commands or match parts



BL=4

SDRAM - Operation

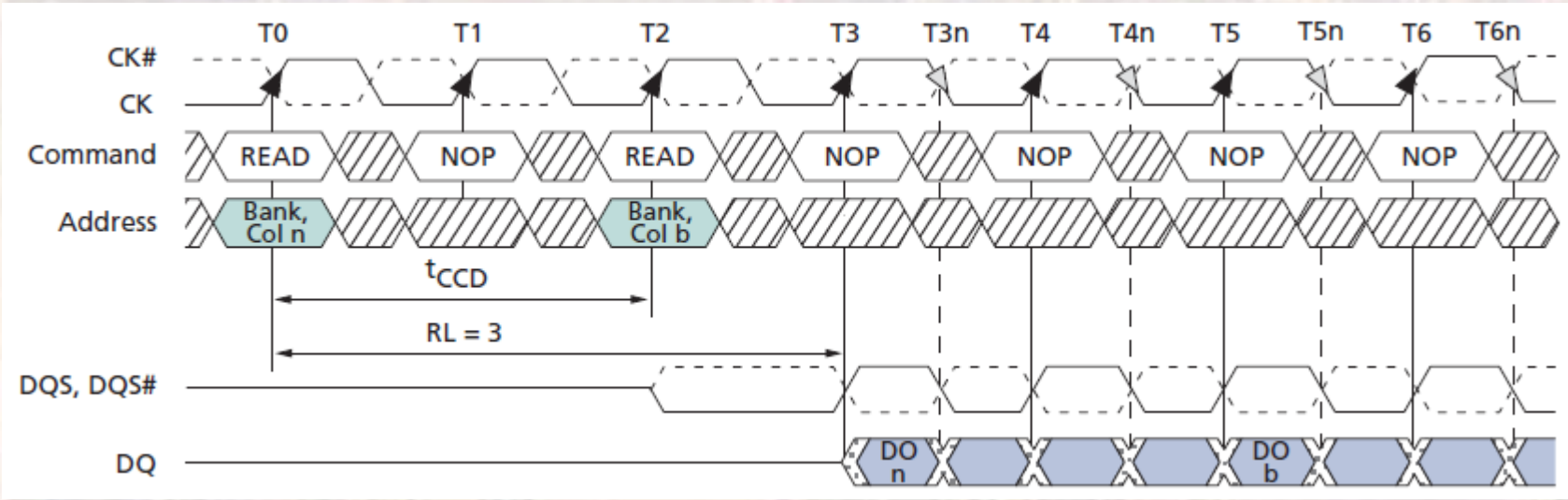
- SDRAM – Timing
  - Non-consecutive Read bursts



BL=4

SDRAM - Operation

- SDRAM – Timing
  - Consecutive Read bursts

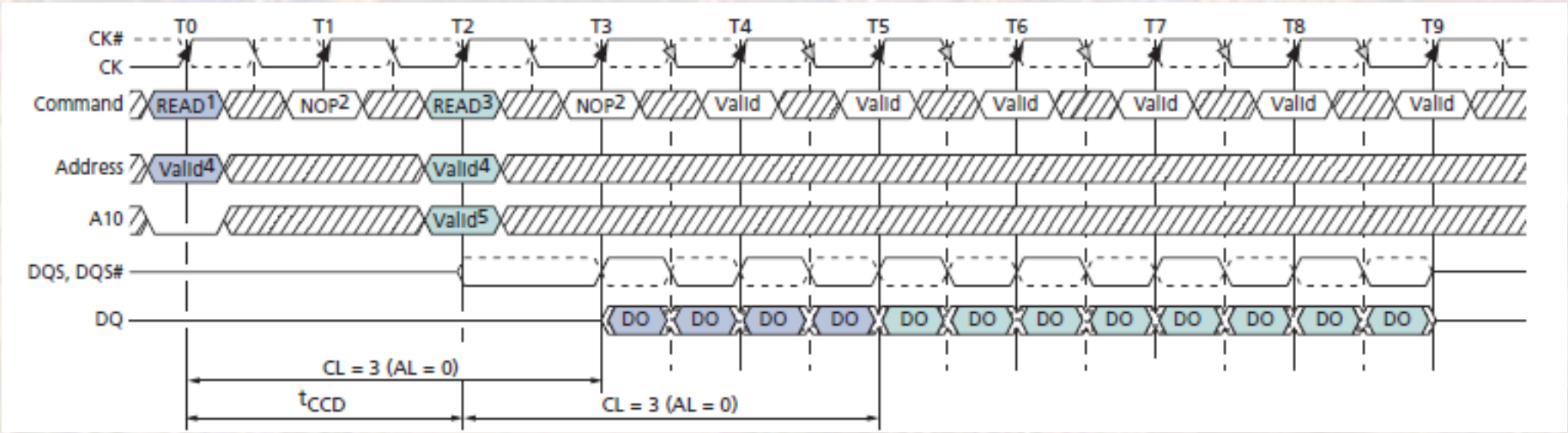


BL=4

SDRAM - Operation

- SDRAM – Timing
  - Read interrupted by read

BL=8

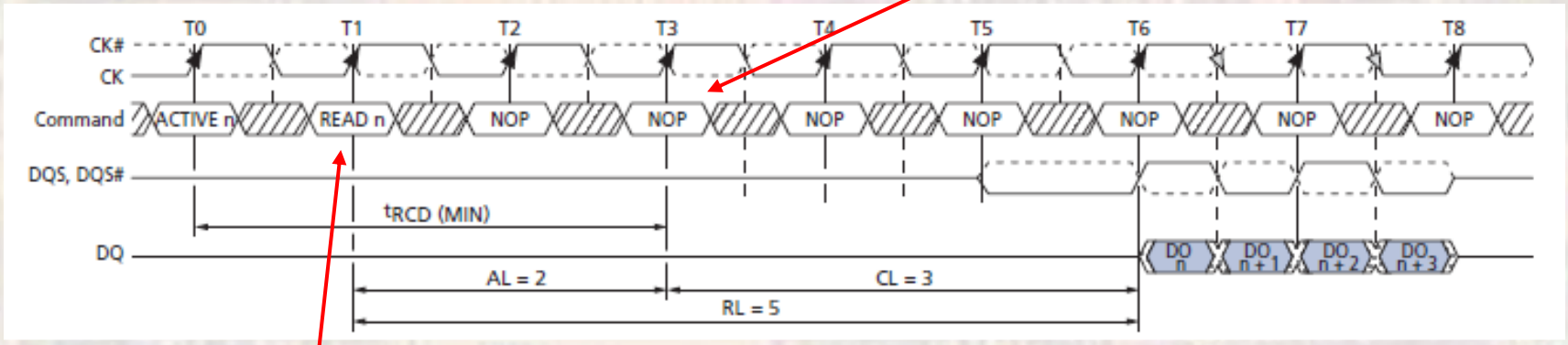


  - Valid addresses include
    - Same bank, same row w/o precharge
    - Different bank – assuming precharged

SDRAM - Operation

- SDRAM – Timing
  - POSTED CAS
    - For CL=3, set AL=2 and move the READ command forward 2 clocks

Normally the read would be here



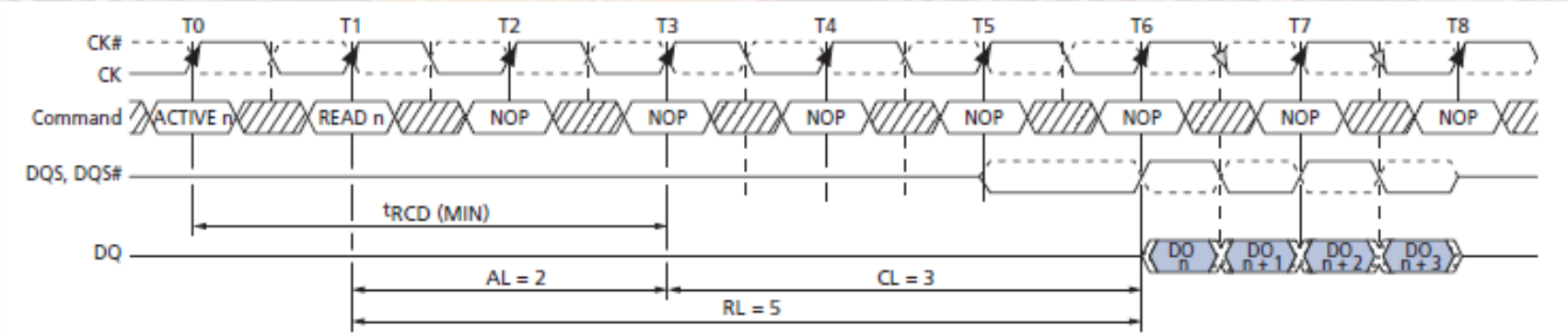
BL=4

Move the read forward to complete the cycle and do something else

SDRAM - Operation

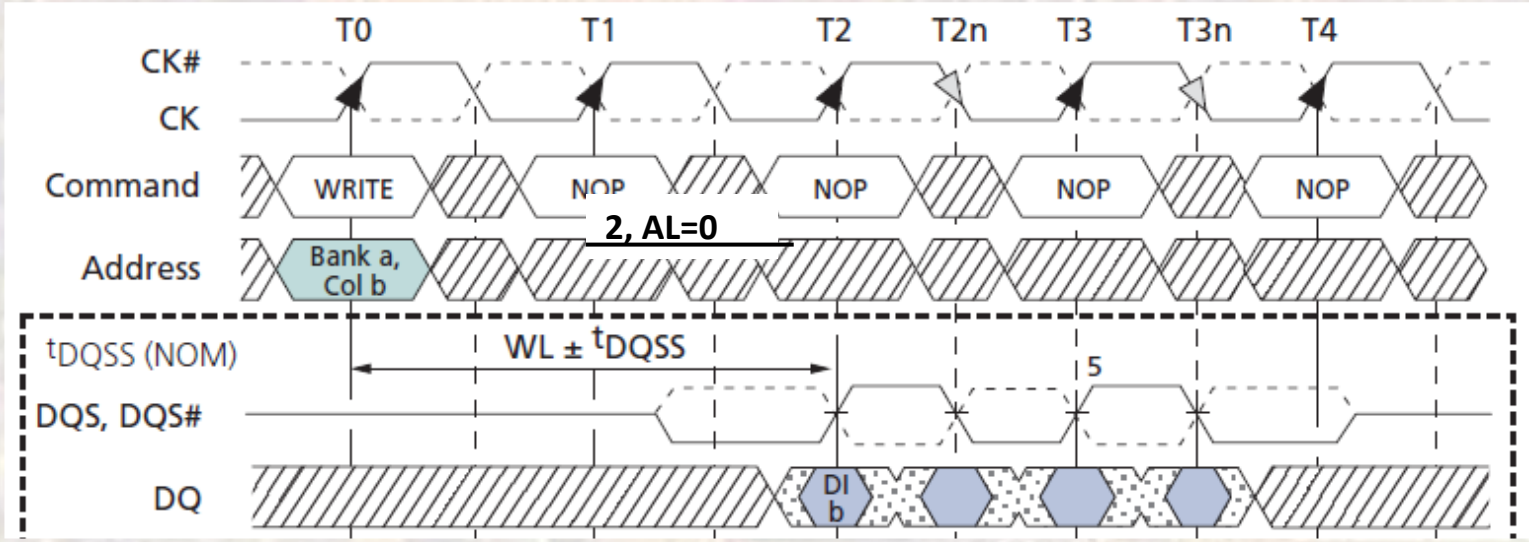
- SDRAM – Timing
  - DQS
    - Signal generated by the SDRAM in read mode
    - Used by the Memory Management Unit (MMU) to know when to sample the read data
    - MMU must sample at halfway point of DQS

BL=4



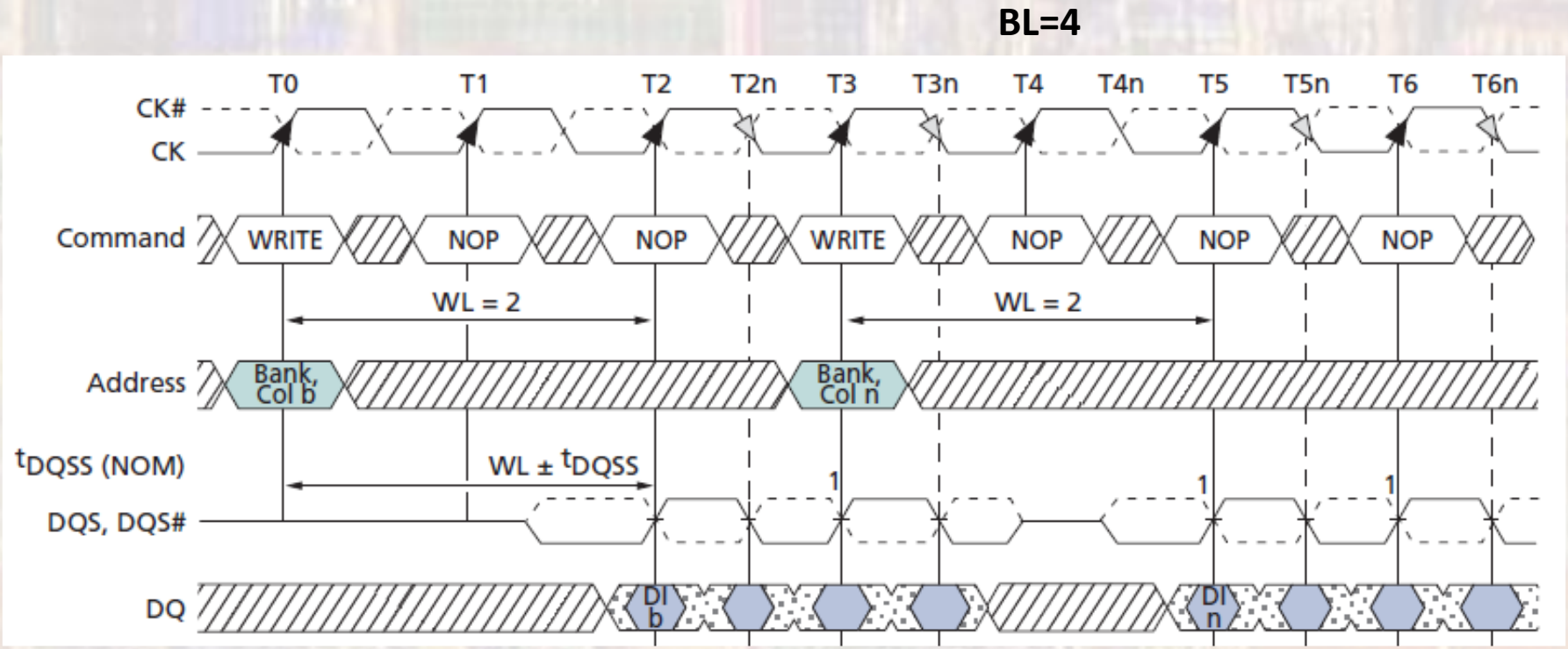
SDRAM - Operation

- SDRAM – Timing
  - Write
    - DQS generated by the MMU in write mode
    - Edge must match up with the center of valid data



SDRAM - Operation

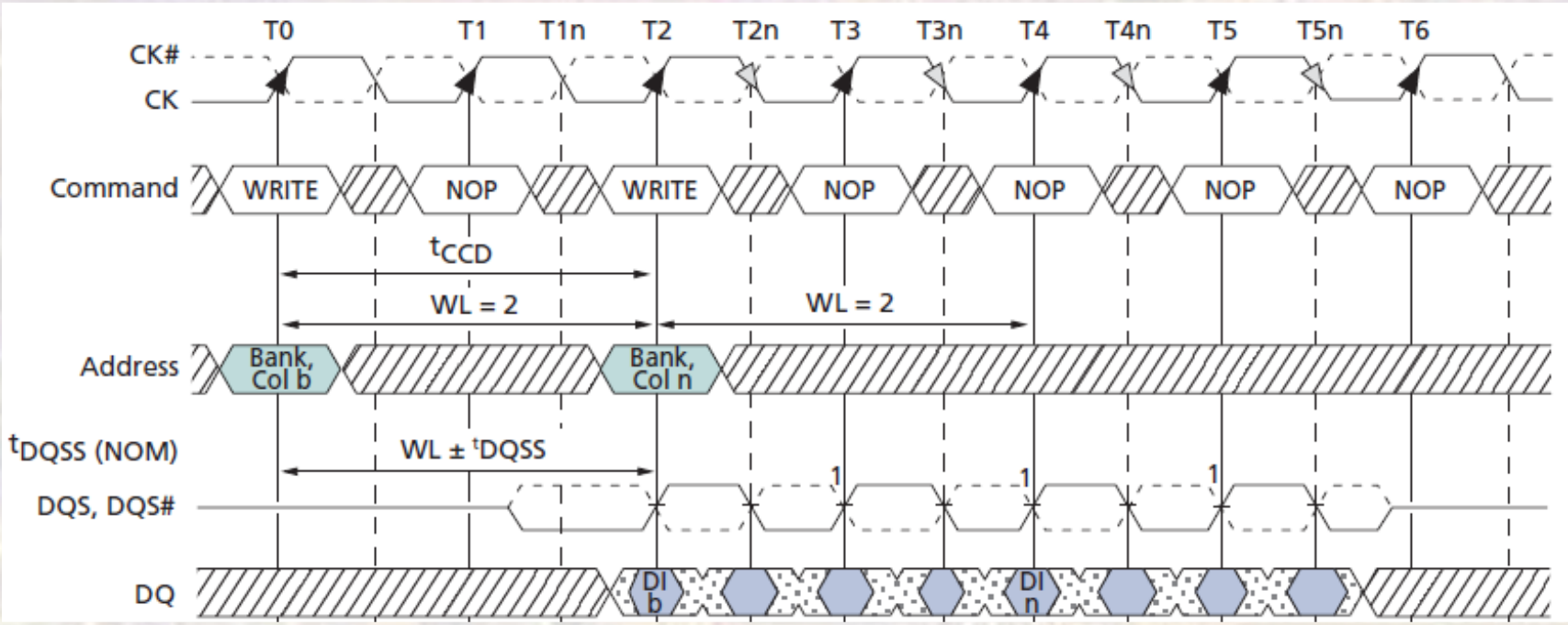
- SDRAM – Timing
  - Non-consecutive Writes



SDRAM - Operation

- SDRAM – Timing
  - Consecutive Writes

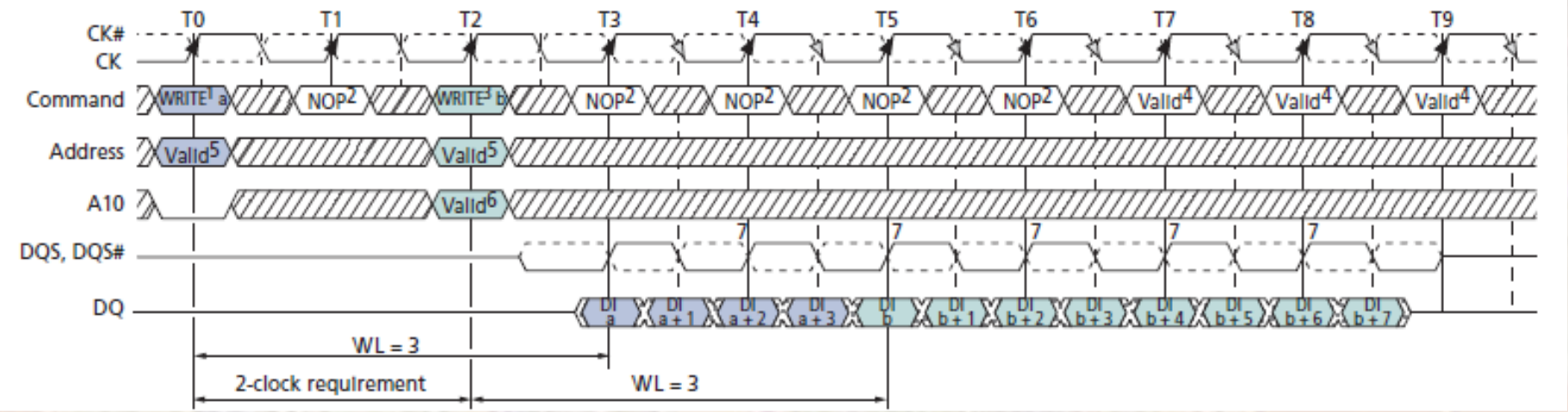
BL=4



SDRAM - Operation

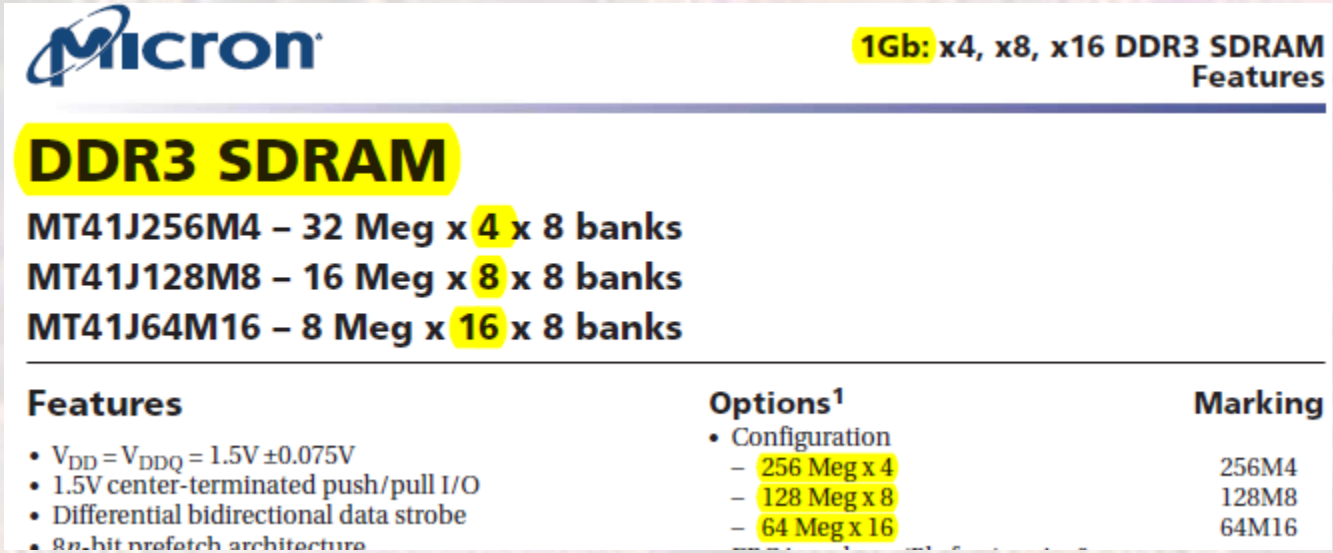
- SDRAM – Timing
  - Write interrupt by Write

BL=8



SDRAM - Operation

- SDRAM – DDR3 spec sheet



Micron

1Gb: x4, x8, x16 DDR3 SDRAM
Features

DDR3 SDRAM

MT41J256M4 – 32 Meg x 4 x 8 banks
MT41J128M8 – 16 Meg x 8 x 8 banks
MT41J64M16 – 8 Meg x 16 x 8 banks

Features

- $V_{DD} = V_{DDQ} = 1.5V \pm 0.075V$
- 1.5V center-terminated push/pull I/O
- Differential bidirectional data strobe
- 8n-bit prefetch architecture

Options[1]

- Configuration
  - 256 Meg x 4
  - 128 Meg x 8
  - 64 Meg x 16

Marking

256M4
128M8
64M16

- 1Gb:x4 = 256Mx4 = 32Mx4x8 same part

- 1Gb = 256Mx4 = 128Mx8 = 64Mx16 different parts
  same die

SDRAM - Operation

- SDRAM – DDR3 spec sheet

Table 1: Key Timing Parameters

Speed Grade	Data Rate (MT/s)	Target ^{t}RCD-^{t}RP-CL	^{t}RCD (ns)	^{t}RP (ns)	CL (ns)
-107[1, 2]	1866	13-13-13	13.91	13.91	13.91
-107E[1, 2]	1866	12-12-12	12.84	12.84	12.84
-125[1, 2]	1600	11-11-11	13.75	13.75	13.75
-15E[1]	1333	9-9-9	13.5	13.5	13.5
187E	1066	7-7-7	13.1	13.1	13.1

- 1866MT/s --> 933MHz clock operation
- --> 1.071ns/clock
- --> CL=13 means tCL = 13.93ns delay

SDRAM - Operation

- SDRAM – DDR3 spec sheet

Table 2: Addressing

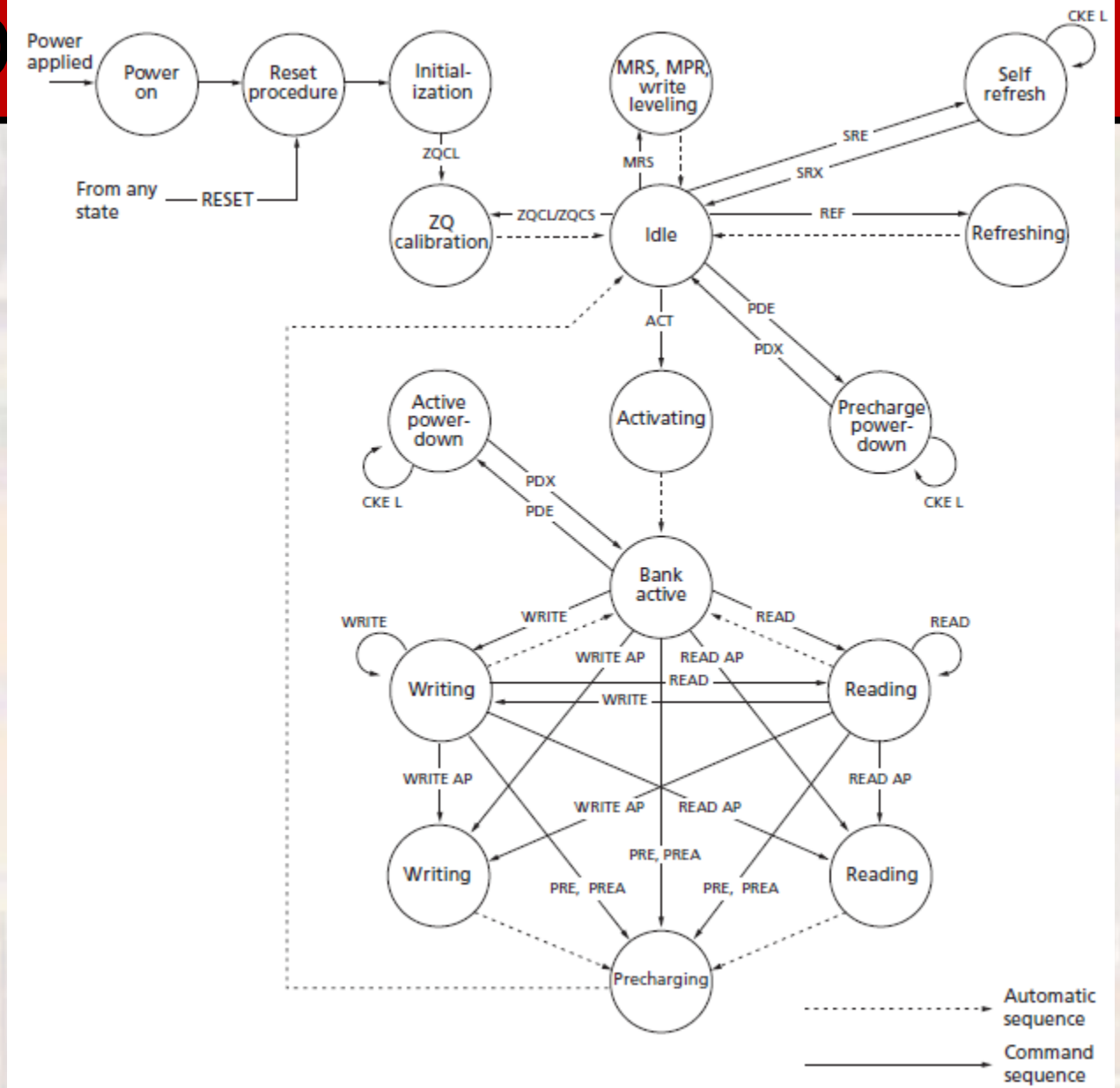
Parameter	256 Meg x 4	128 Meg x 8	64 Meg x 16
Configuration	32 Meg x 4 x 8 banks	16 Meg x 8 x 8 banks	8 Meg x 16 x 8 banks
Refresh count	8K	8K	8K
Row addressing	16K (A[13:0])	16K (A[13:0])	8K (A[12:0])
Bank addressing	8 (BA[2:0])	8 (BA[2:0])	8 (BA[2:0])
Column addressing	2K (A[11, 9:0])	1K (A[9:0])	1K (A[9:0])
Page Size	1KB	1KB	2KB

- It appears this memory has
  - 8 arrays
  - 8K rows X 16K bitlines 8 X 8K X 16Kb = 1Gb
  - x4 and x8 break rows in half
  - x4 halves the column

SDRAM - O

- SDRAM – DDR3 spec sheet

Figure 2: Simplified State Diagram



SDRAM - Operation

- SDRAM – DDR3 spec sheet

Table 70: Truth Table – Command

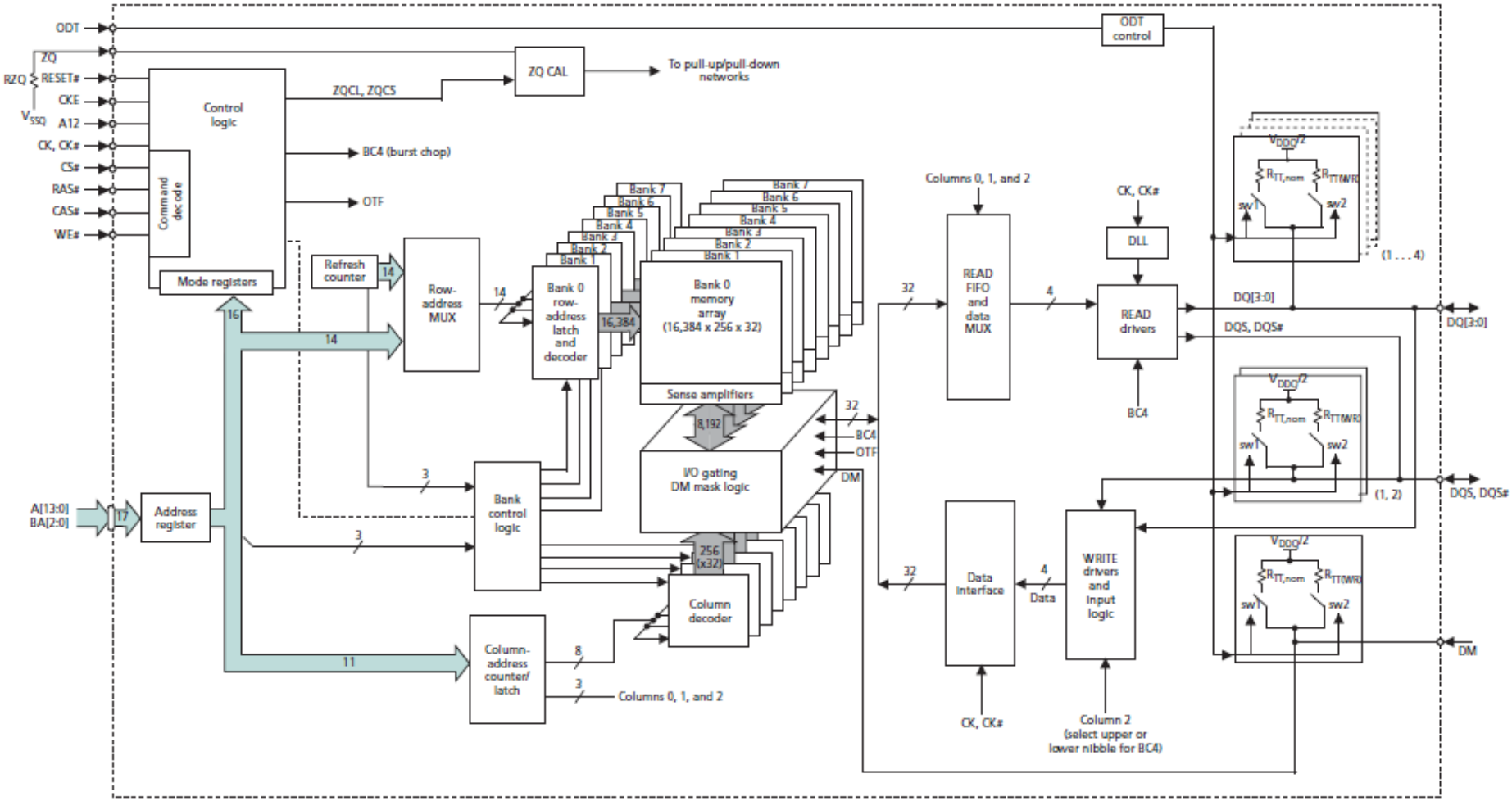
Notes 1–5 apply to the entire table

Function	Symbol	CKE		CS#	RAS#	CAS#	WE#	BA [2:0]	An	A12	A10	A[11, 9:0]	Notes
		Prev. Cycle	Next Cycle										
Bank ACTIVATE	ACT	H	H	L	L	H	H	BA	Row address (RA)				
WRITE BL8MRS,	WR	H	H	L	H	L	L	BA	RFU	V	L	CA	8
READ BL8MRS,	RD	H	H	L	H	L	H	BA	RFU	V	L	CA	8
Single-bank PRECHARGE	PRE	H	H	L	L	H	L	BA	V	V	L	V	
PRECHARGE all banks	PREA	H	H	L	L	H	L	V		V	H	V	

SDRAM - Operation

- SDRAM – DDR3 spec sheet

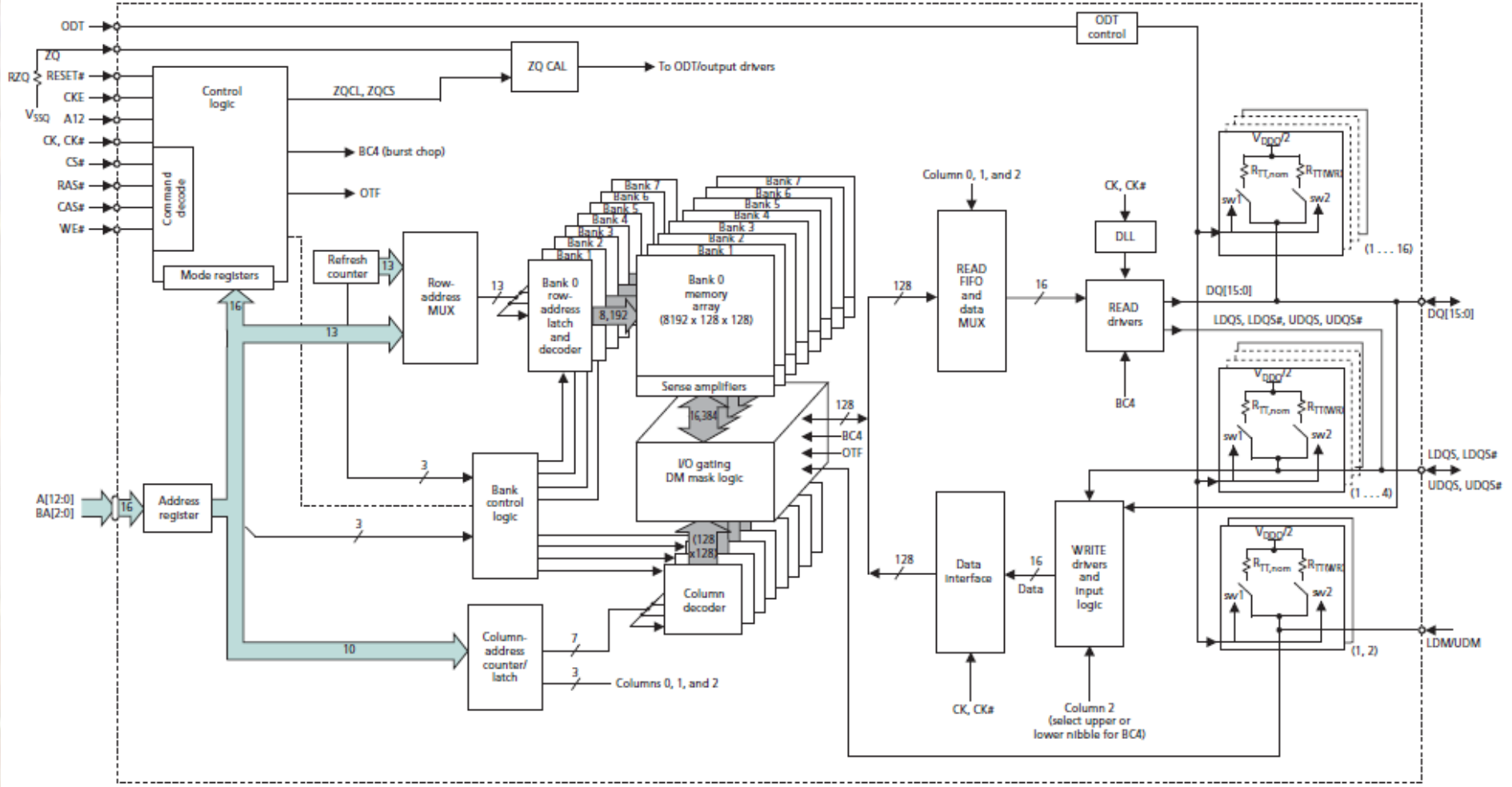
Figure 3: 256 Meg x 4 Functional Block Diagram



SDRAM - Operation

- SDRAM – DDR3 spec sheet

Figure 5: 64 Meg x 16 Functional Block Diagram

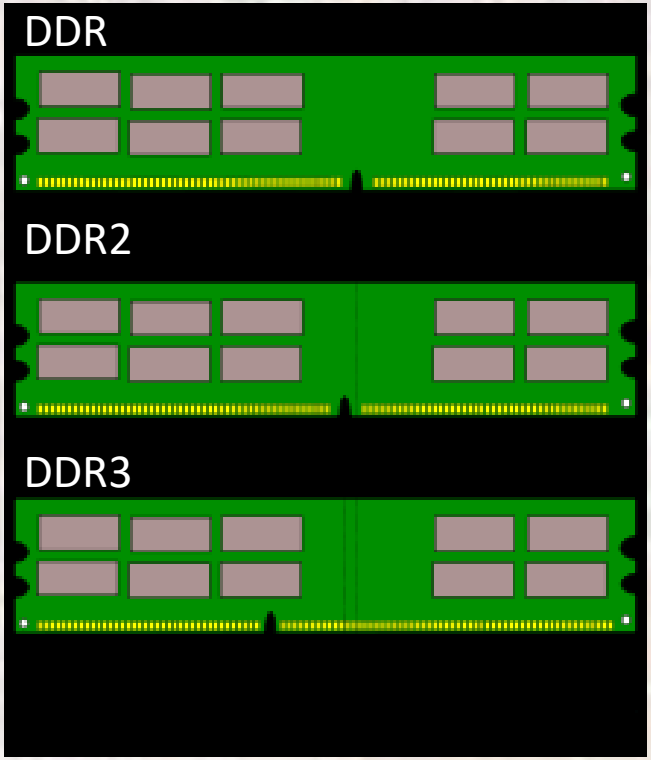


SDRAM - Operation

- Dimm
  - Dual Inline Memory Module
  - Multiple memory chips integrated onto a board
  - Support 64bit transfers
  - Parallel configuration
    - Different chip selects
  - Word configuration
    - Each chip supplies part of a bigger word
    - 8, x1 devices → 8 bit word
    - 8, x4 devices → 32 bit word
  - use PCx-zzzz where zzzz is max bandwidth (transfer rate in bytes)
    - DDR2-800 → pc2-6400 (transfers x # bits /8) = 800M x 64b /8 = 6.4GB/s

SDRAM - Operation

- Dimm
  - pc, pc2, pc3 – different slot configurations



SDRAM - Operation

- DDR - Technology

Technology	Typical Voltage
DDR	2.5 V
DDR2	1.8 V
DDR3	1.5 V
DDR4	1.2 V
DDR5	1.1 V

Memory	Real Clock	Maximum Theoretical Transfer Rate	Memory Module
DDR200	100 MHz	1,600 MB/s	PC-1600
DDR266	133 MHz	2,133 MB/s	PC-2100
DDR333	166 MHz	2,666 MB/s	PC-2700
DDR400	200 MHz	3,200 MB/s	PC-3200
DDR2-400	200 MHz	3,200 MB/s	PC2-3200
DDR2-533	266 MHz	4,266 MB/s	PC2-4200
DDR2-667	333 MHz	5,333 MB/s	PC2-5300
DDR2-800	400 MHz	6,400 MB/s	PC2-6400
DDR2-1066	533 MHz	8,533 MB/s	PC2-8500
DDR3-800	400 MHz	6,400 MB/s	PC3-6400
DDR3-1066	533 MHz	8,500 MB/s	PC3-8500
DDR3-1333	666 MHz	10,666 MB/s	PC3-10600
DDR3-1600	800 MHz	12,800 MB/s	PC3-12800

SDRAM - Operation

- DDR – Technology
  - DDR4

Standard name	Memory clock (MHz)	I/O bus clock (MHz)	Data rate (MT/s)	Module name	Peak transfer rate (MB/s)	Timings CL-tRCD-tRP	CAS latency (ns)
DDR4-1600J* DDR4-1600K DDR4-1600L	200	800	1600	PC4-12800	12800	10-10-10 11-11-11 12-12-12	12.5 13.75 15
DDR4-1866L* DDR4-1866M DDR4-1866N	233.33	933.33	1866.67	PC4-14900	14933.33	12-12-12 13-13-13 14-14-14	12.857 13.929 15
DDR4-2133N* DDR4-2133P DDR4-2133R	266.67	1066.67	2133.33	PC4-17000	17066.67	14-14-14 15-15-15 16-16-16	13.125 14.063 15
DDR4-2400P* DDR4-2400R DDR4-2400T DDR4-2400U	300	1200	2400	PC4-19200	19200	15-15-15 16-16-16 17-17-17 18-18-18	12.5 13.32 14.16 15
DDR4-2666T DDR4-2666U DDR4-2666V DDR4-2666W	333.33	1333.33	2666.67	PC4-21333	21333.33	17-17-17 18-18-18 19-19-19 20-20-20	12.75 13.50 14.25 15
DDR4-2933V DDR4-2933W DDR4-2933Y DDR4-2933AA	366.67	1466.67	2933.33	PC4-23466	23466.67	19-19-19 20-20-20 21-21-21 22-22-22	12.96 13.64 14.32 15
DDR4-3200W DDR4-3200AA DDR4-3200AC	400	1600	3200	PC4-25600	25600	20-20-20 22-22-22 24-24-24	12.5 13.75 15

SDRAM - Operation

- DDR – Technology
  - DDR5

Feature	DDR5 DRAMs	DDR4 DRAMs
Device size	8Gb to 64Gb	2Gb to 16Gb
Speed	Up to 6400 Mbps	Up to 3200 Mbps
Voltage	1.1V DRAM I/O	1.2V DRAM I/O
Burst length per transaction	16 beats	8 beats
DIMM topology	• Dual-channel, with each channel being 32-bits wide for data • ECC DIMMs are generally 80-bits wide, with 40 bits per channel	• Single-channel with a data-width of 64 bits • ECC DIMMs are 72-bits wide