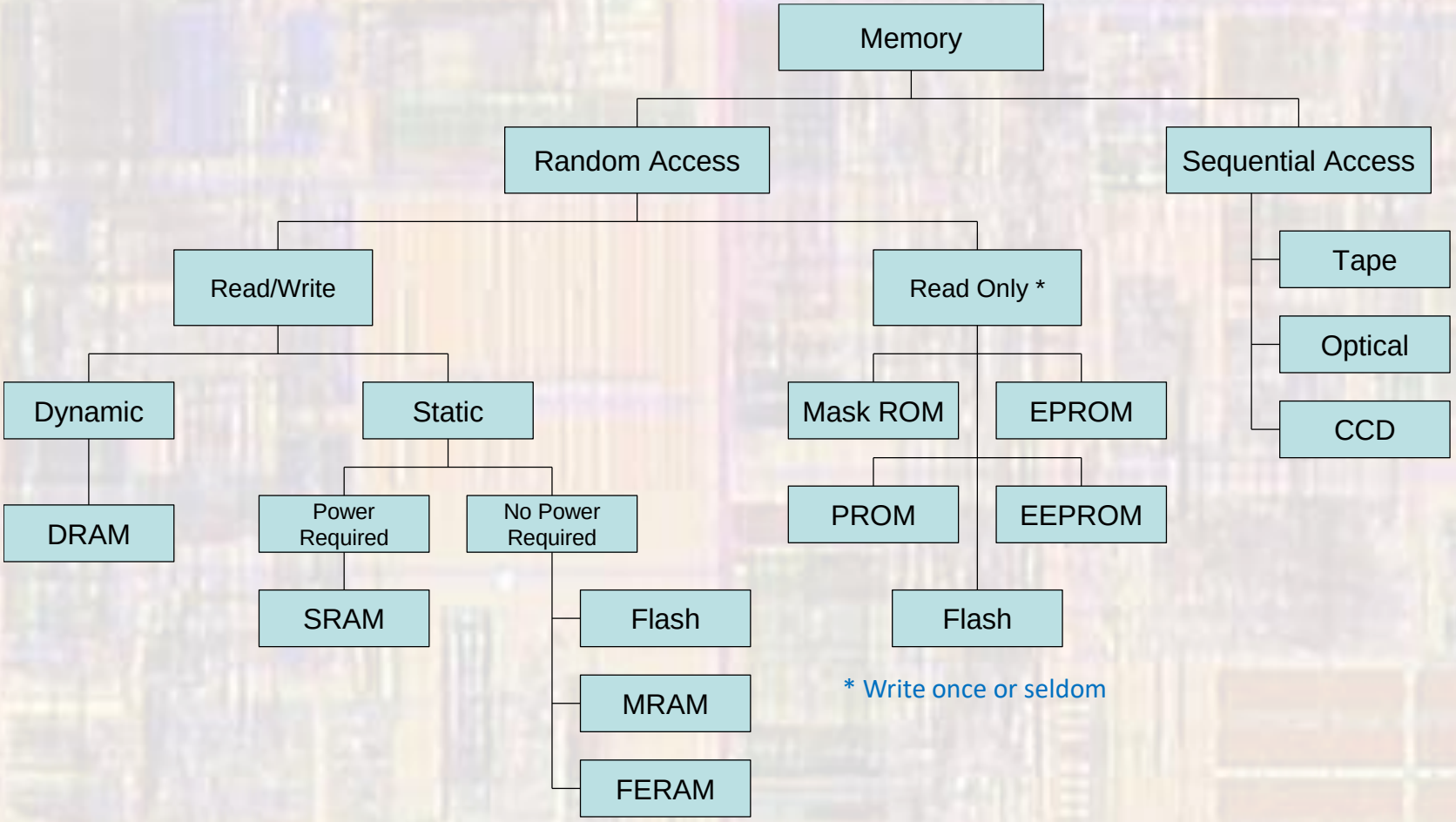
# SRAM

Last updated 4/28/22

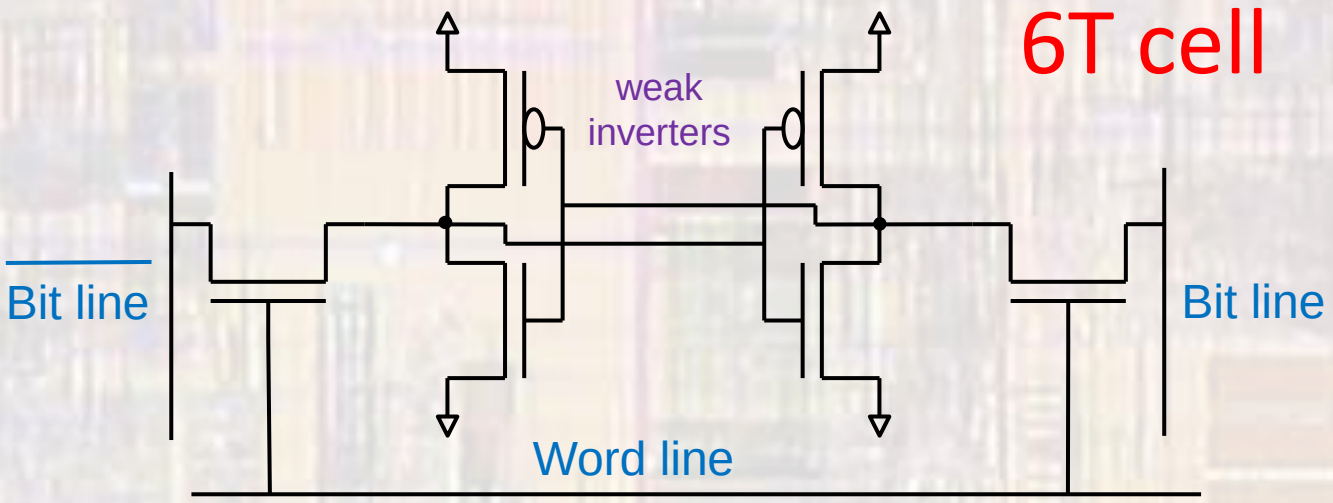
# Memory - SRAM

- Memory Taxonomy



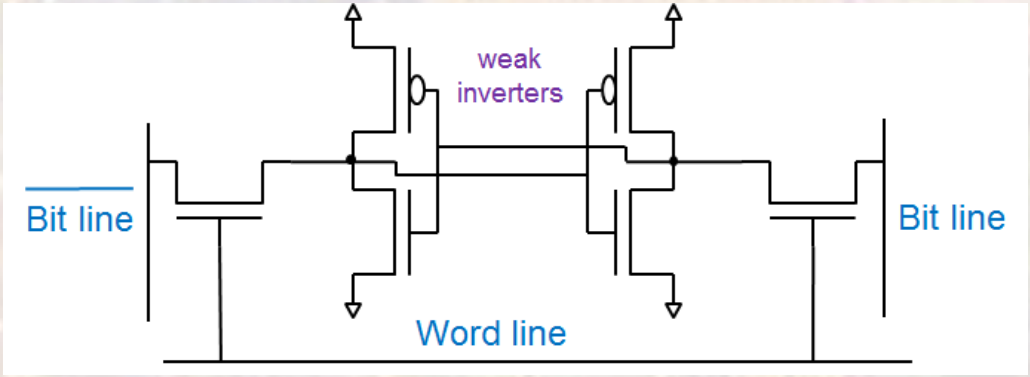
# Memory - SRAM

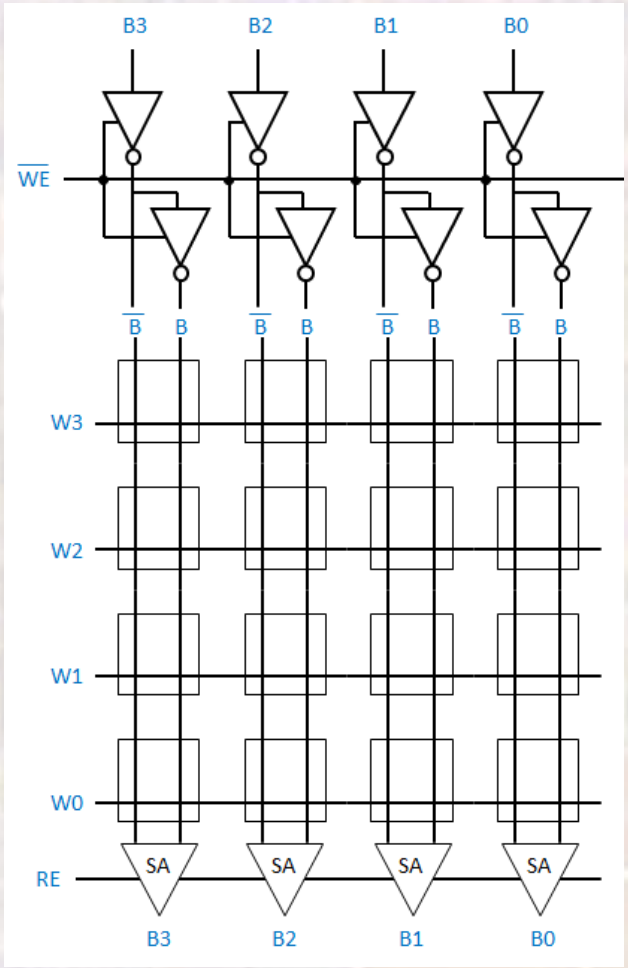
- SRAM – Static Random Access Memory
  - Memory cell (1 bit) is based on a feedback circuit
  - Bit value is retained as long as power is maintained
  - Fastest read/write (R/W)
  - Highest power
  - Lowest density
  - Used in caches and small data memories



# Memory - SRAM

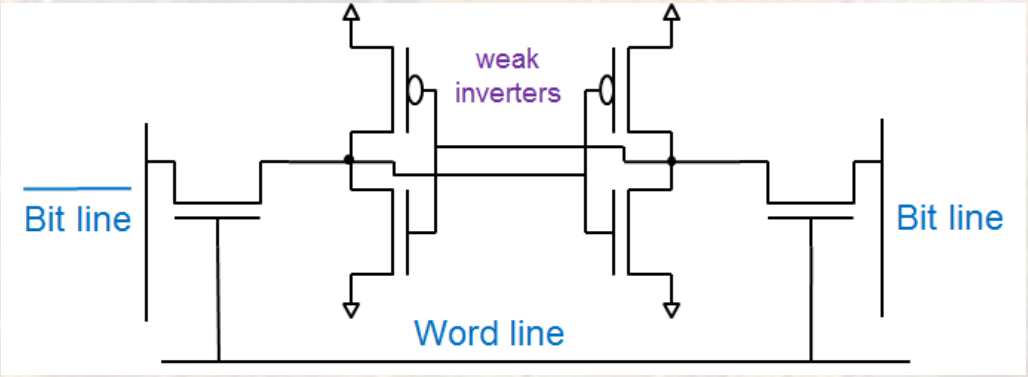
- SRAM – Static Random Access Memory
  - Write
    - All Word lines low
    - Read Enable (RE) disabled (low)
    - Place B0, B1, B2, B3 on inputs
    - Pull write enable bar ($\overline{WE}$) low
    - Strobe the desired word line high
    - Bit lines override the bit cell inverters and store the new value in the cell

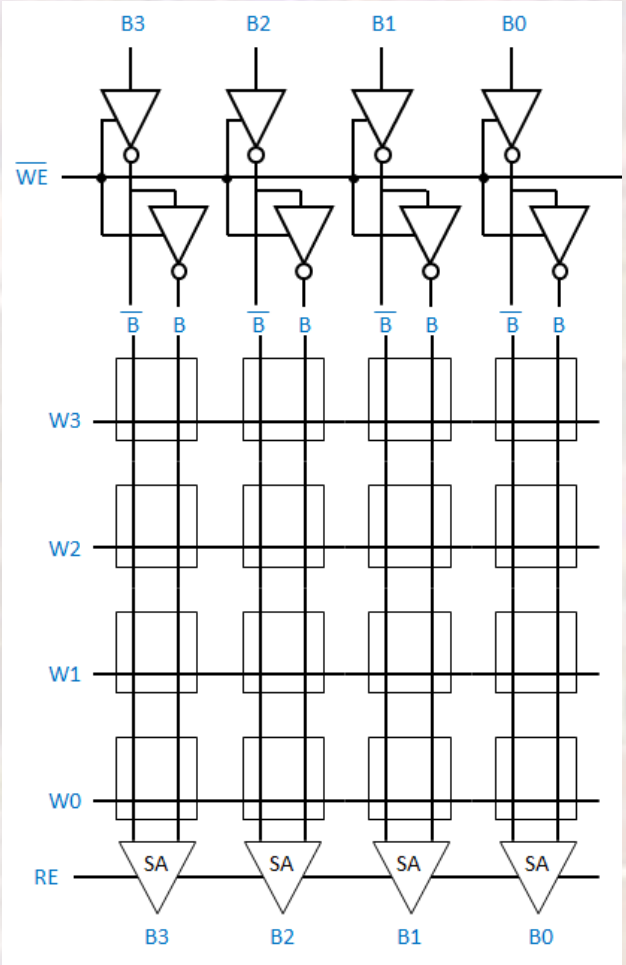


# Memory - SRAM

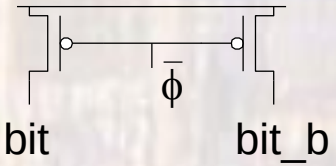
- SRAM – Static Random Access Memory
  - Read
    - All Word lines low
    - Write enable bar ($\overline{WE}$) high
      - inverters tristated
    - Read Enable (RE) high
    - Strobe the desired word line high
    - Bit cell inverters drive the bit lines and sense amplifiers read the value



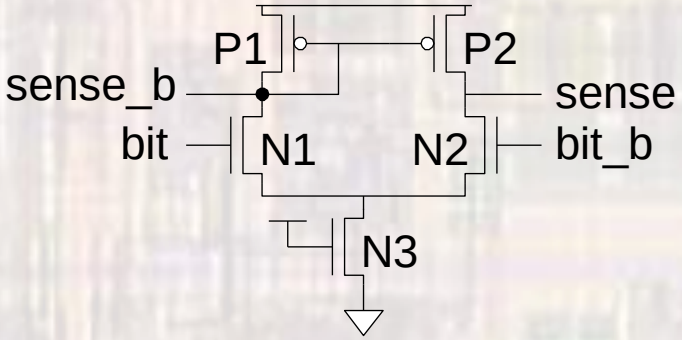



# Memory - SRAM

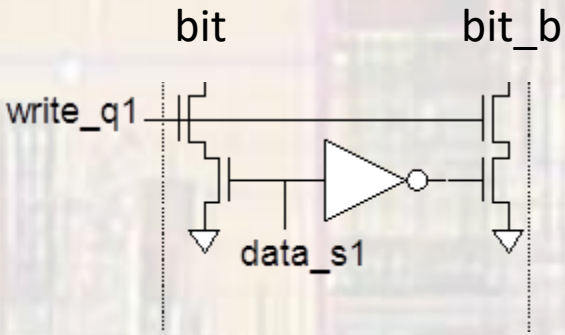
- SRAM – Static Random Access Memory
  - Pre-charging
    - To ensure consistent timing pre-charge bit and bit_b




- Sense amplifier
  - With large arrays, the bit/bit_b transition times can be very long
  - Use high gain sense amplifiers to make decisions quickly

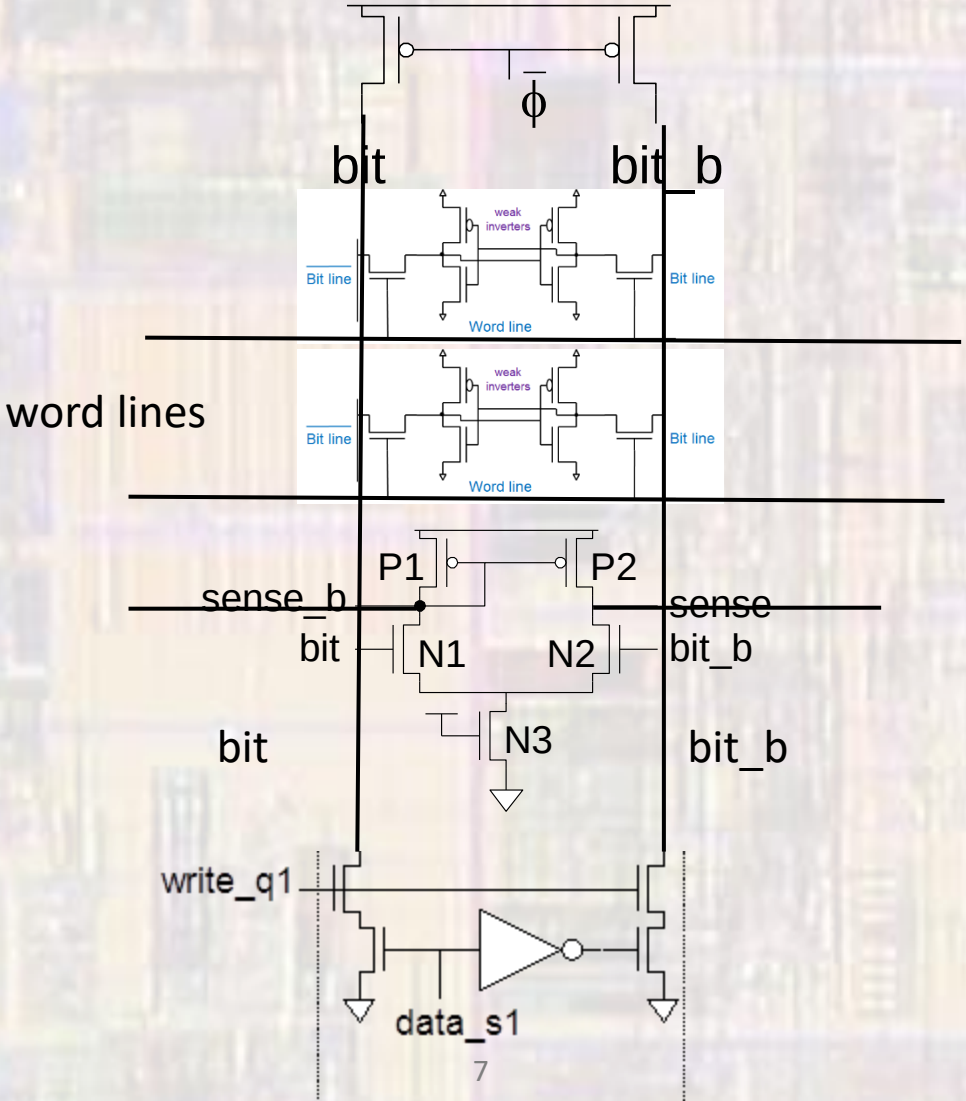



- Write Enable



# Memory - SRAM

- SRAM



# Memory - SRAM

- SRAM – Static Random Access Memory
  - Circuit timing