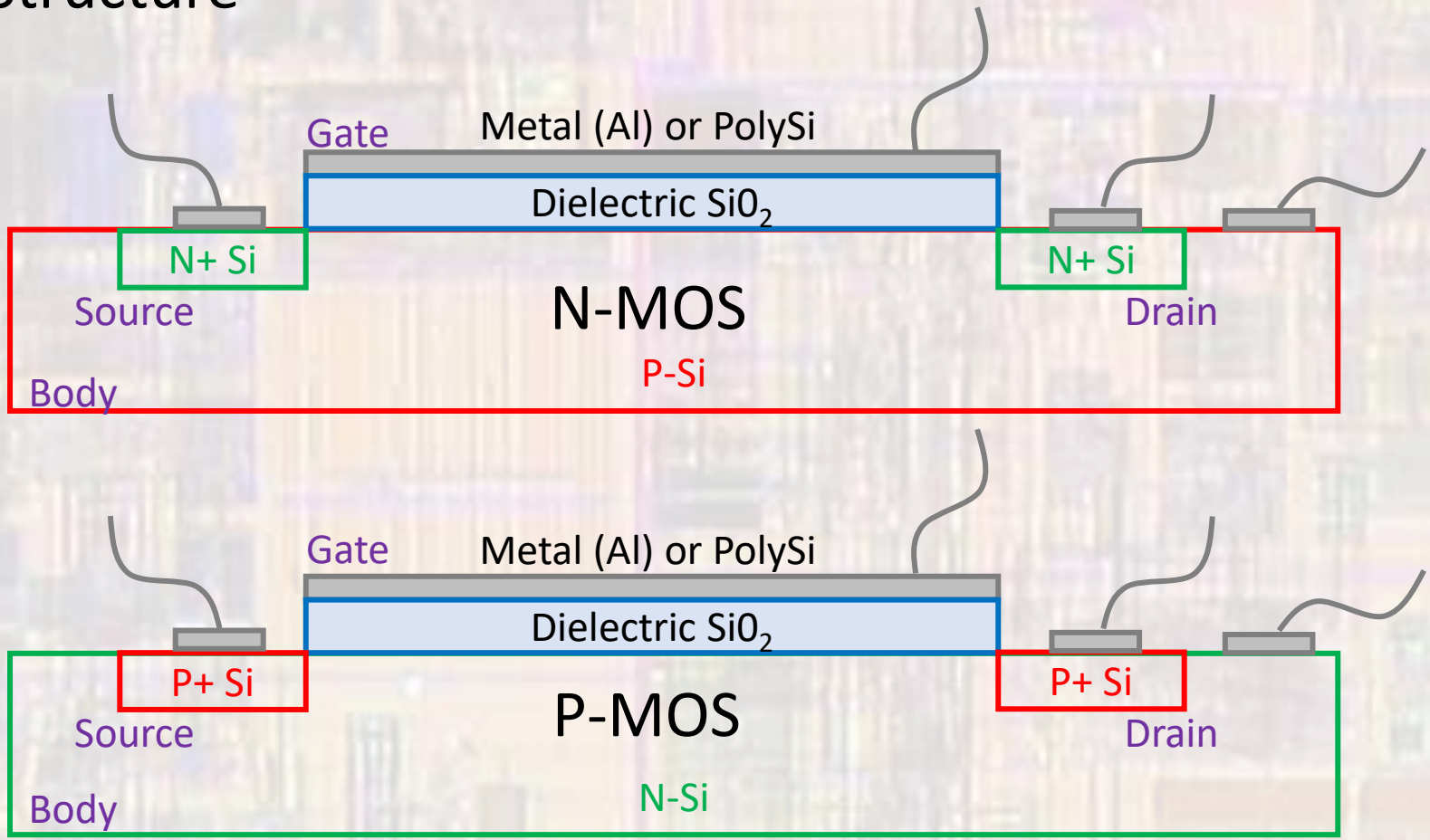
Metal Oxide Semiconductor Enhancement Mode Transistor

Last updated 3/24/22

MOS Enhancement Mode Transistor

- Structure



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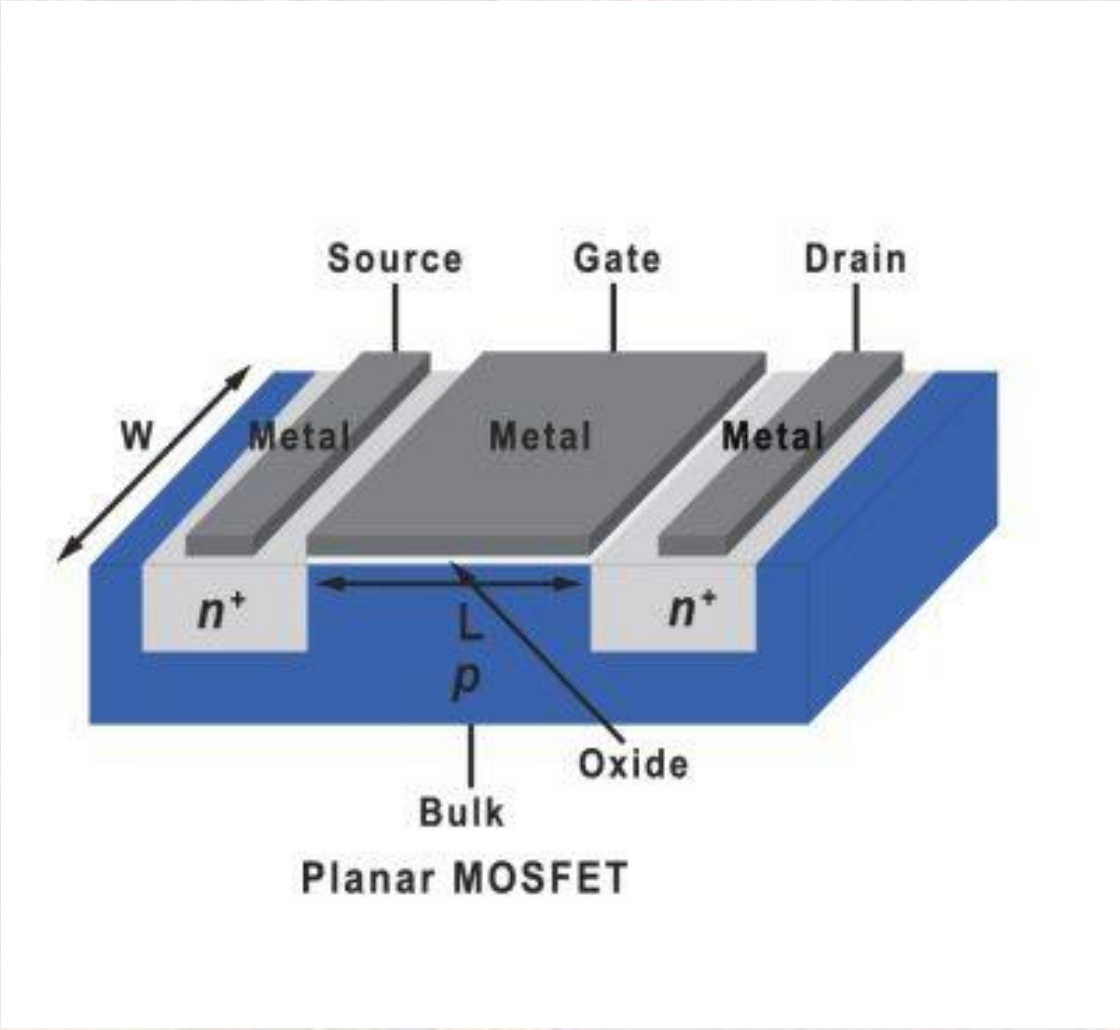
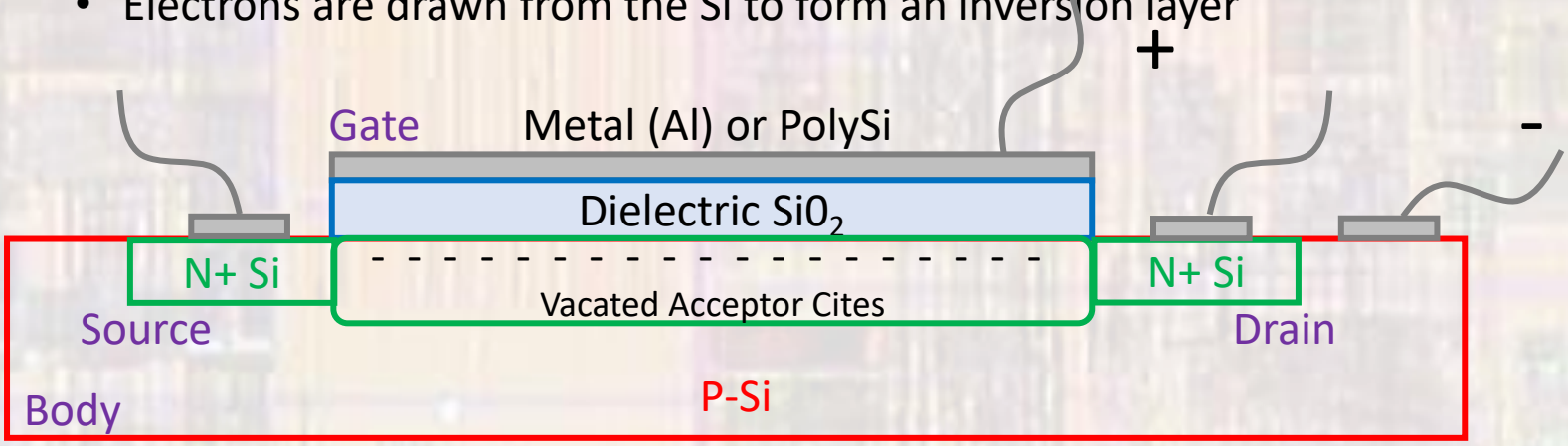
- Structure



MOS Enhancement Mode Transistor

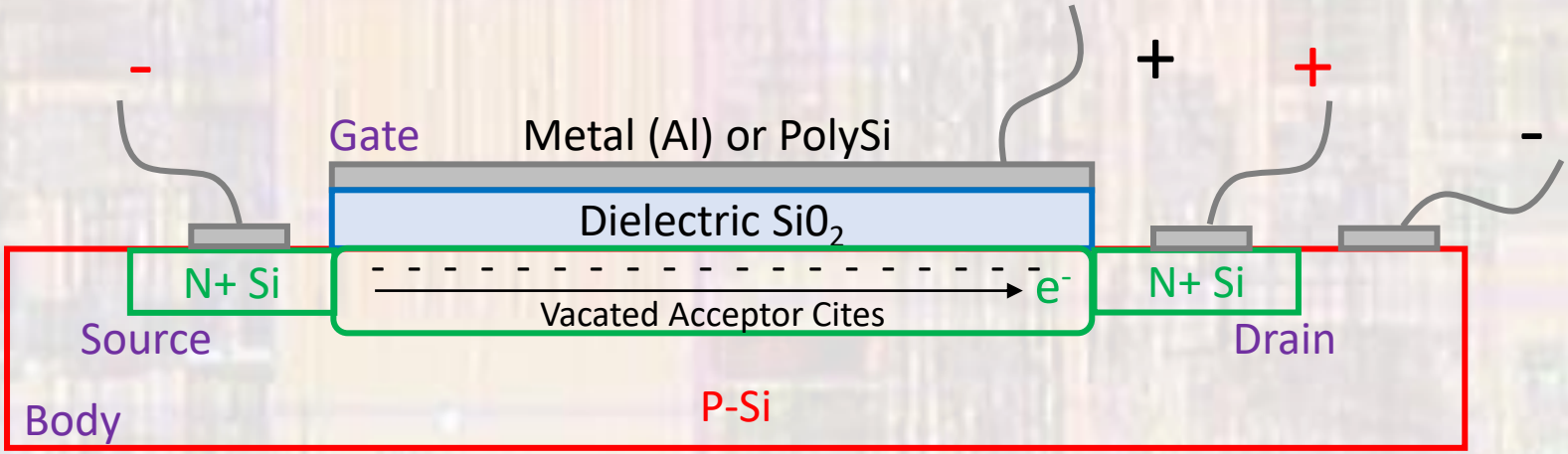
- N-MOS Operation
  - Large Positive Bias
    - Depletion region is formed
      - Mobile holes pushed away (region is depleted of holes)
      - Net negative (fixed) charge left behind
      - Electrons are drawn from the Si to form an inversion layer



A channel is formed from Source to Drain
Electrons can flow through this channel

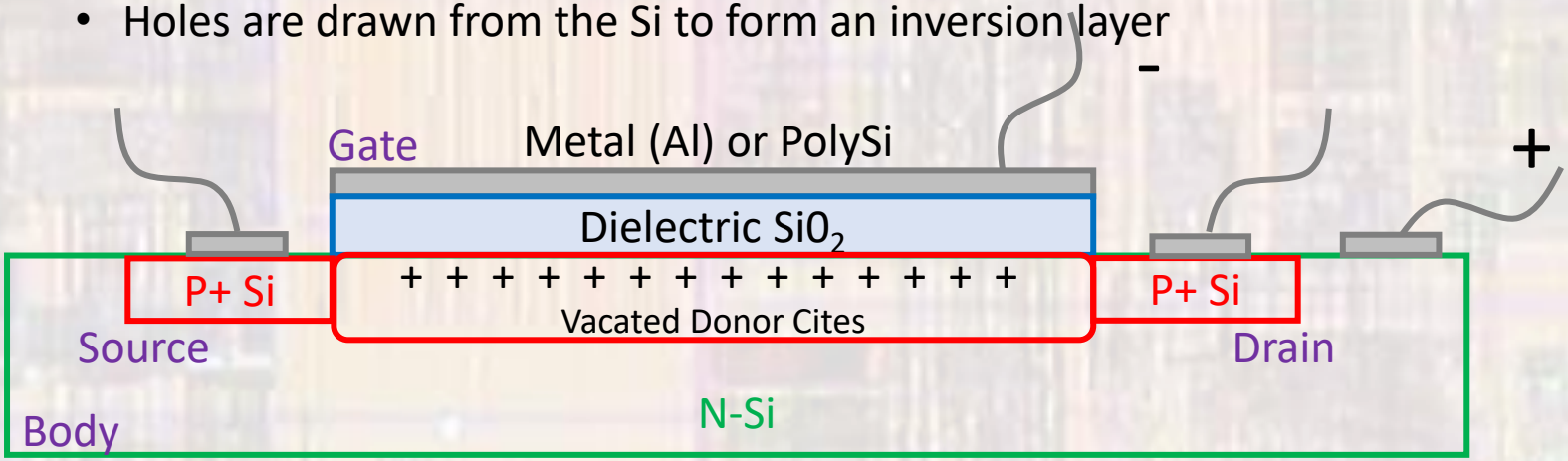
MOS Enhancement Mode Transistor

- N-MOS Operation
  - Large Positive Bias + Positive Bias from Drain to Source
    - Electrons move from Source to Drain
    - Current flows from Drain to Source



MOS Enhancement Mode Transistor

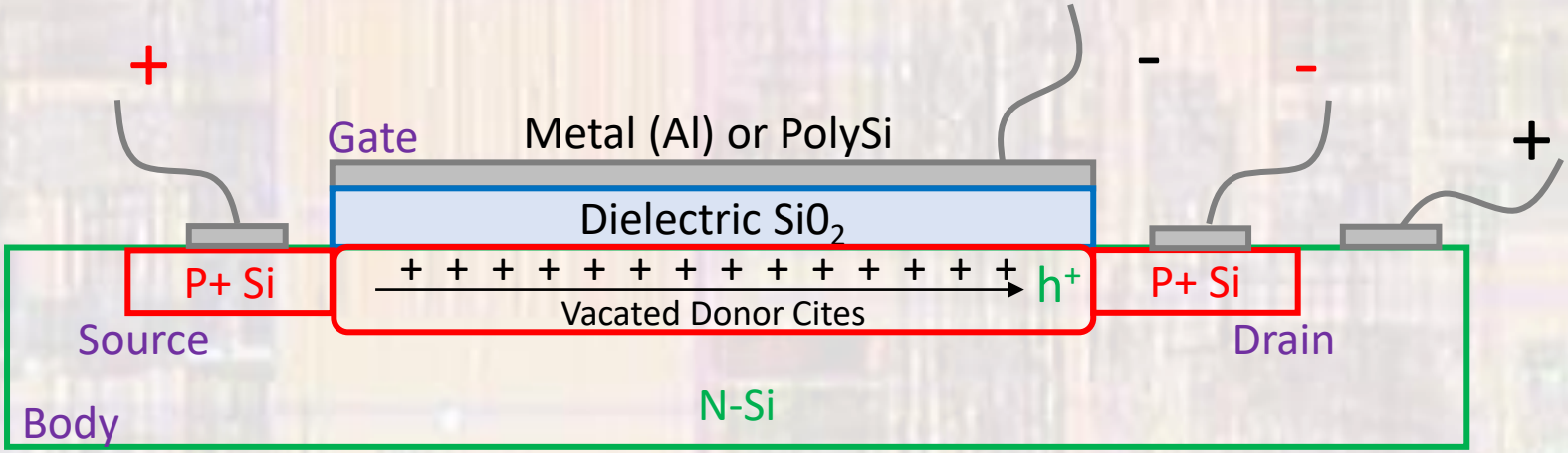
- P-MOS Operation
  - Large Negative Bias
    - Depletion region is formed
      - Mobile electrons pushed away (region is depleted of electrons)
      - Net positive (fixed) charge left behind
      - Holes are drawn from the Si to form an inversion layer



A channel is formed from Source to Drain
Holes can flow through this channel

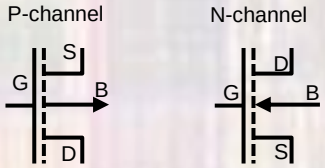
MOS Enhancement Mode Transistor

- P-MOS Operation
  - Large Negative Bias + Positive Bias from Source to Drain
    - Holes move from Source to Drain
    - Current flows from Source to Drain

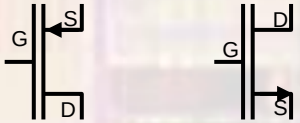


MOS Enhancement Mode Transistor

- Enhancement Mode
  - A bias is required to form the channel
  - 4-terminal symbol



  - In digital applications the Source is typically tied to
    - Vdd for P-MOS
    - Gnd for N-MOS



  - The simplified logic symbols

Note – almost all N-MOS and P-MOS devices used today are enhancement mode – so the dashed line is omitted

MOS Enhancement Mode Transistor

- Parameters
  - W – width of the transistor
  - L – length of the transistor (S to D)
  - V_{th} – threshold voltage (inversion layer formed)
  - Kn, Kp – conduction parameter

$$K_n = \frac{W \mu_n C_{ox}}{2L} \qquad K_p = \frac{W \mu_p C_{ox}}{2L}$$

$$K_n = \frac{k_n'}{2}\frac{W}{L} \qquad K_p = \frac{k_p'}{2}\frac{W}{L}$$

$$k_n' = \mu_n C_{ox} \qquad k_p' = \mu_p C_{ox}$$

μ_n, μ_n, C_{ox} fixed for a given semiconductor process