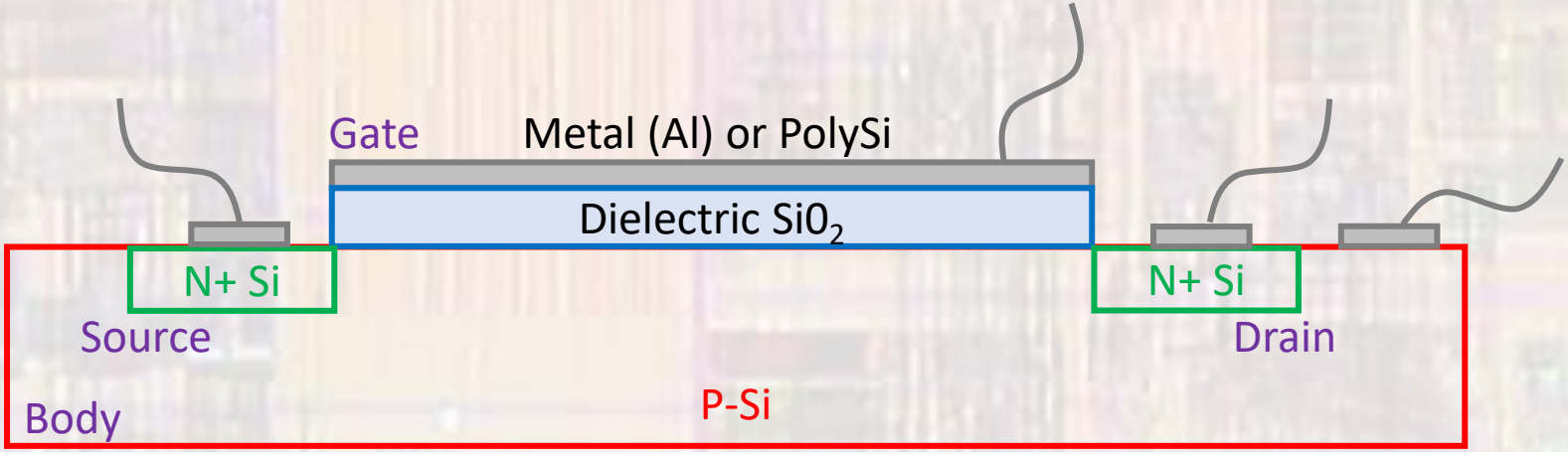
MOS I-V Characteristics

Last updated 3/25/22

MOS I-V Characteristics

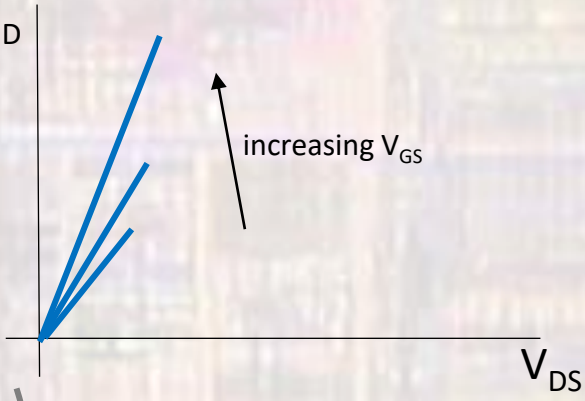
- N-MOS Operation - Cutoff
  - $V_{GS} < V_{th}$
    - No inversion region is formed
      - No electrons flow from source to drain
      - No current flow from drain to source

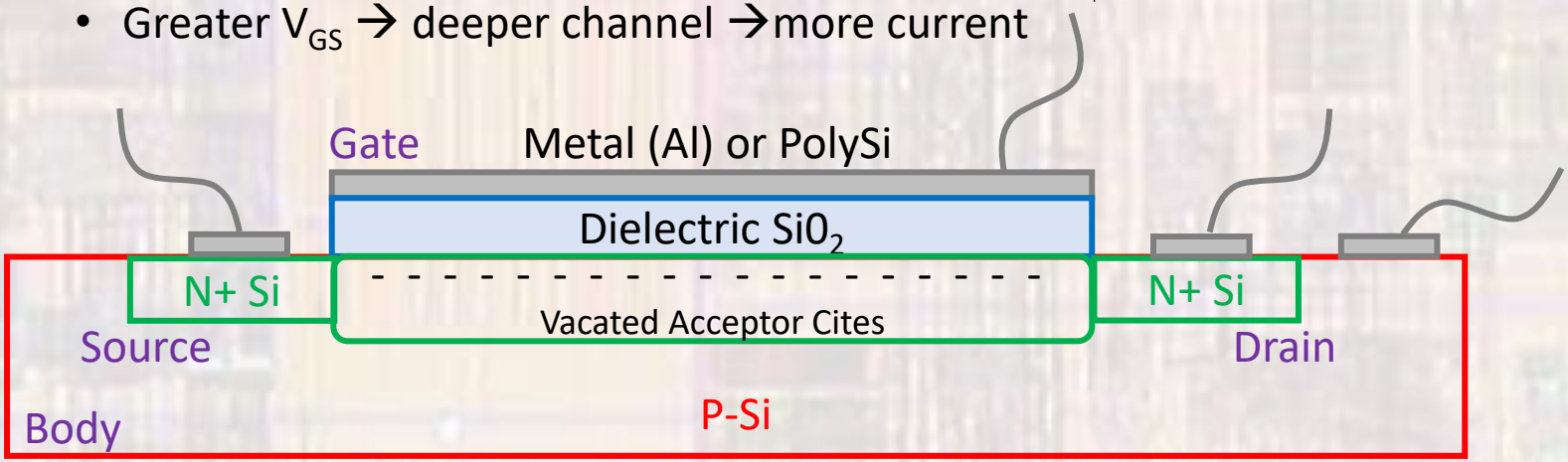


$$I_D = 0$$

MOS I-V Characteristics

- N-MOS Operation – non-saturation
  - $V_{GS} > V_{th}$
    - Inversion region is formed
      - Electrons can flow from source to drain
      - Current can flow from drain to source
      - Greater V_{GS} → deeper channel →more current

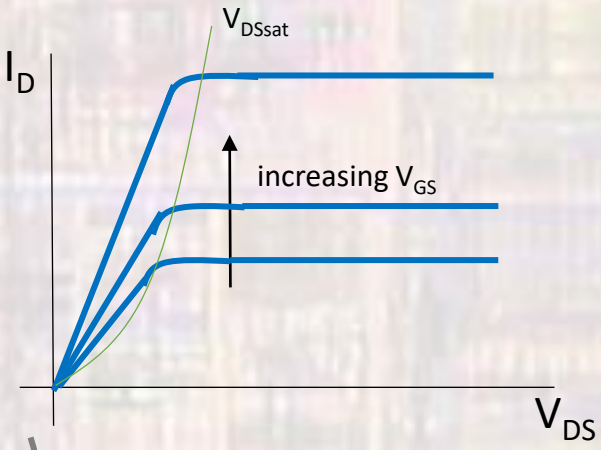


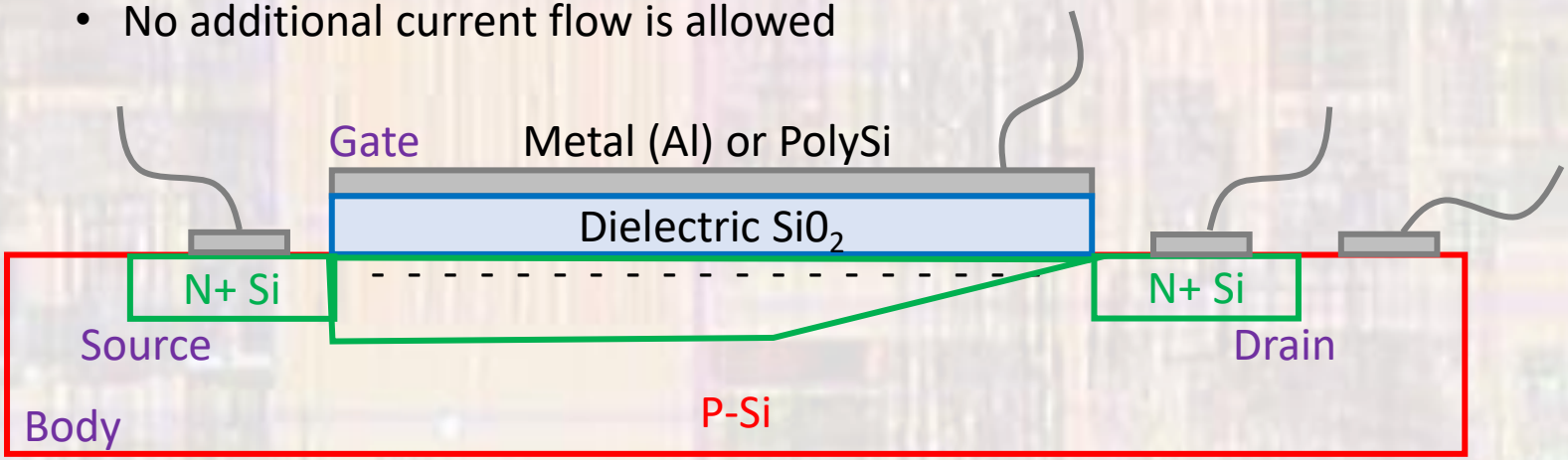


$$I_D = K_n[2(V_{GS} - V_{tn})V_{DS} - V_{DS}^2]$$

MOS I-V Characteristics

- N-MOS Operation – saturation
  - $V_{GS} > V_{th}$, $V_{DS} > V_{DSsat}$
    - Inversion region is formed
      - V_D is high enough to counteract the V_G near the drain → "pinch-off" of the channel
      - No additional current flow is allowed



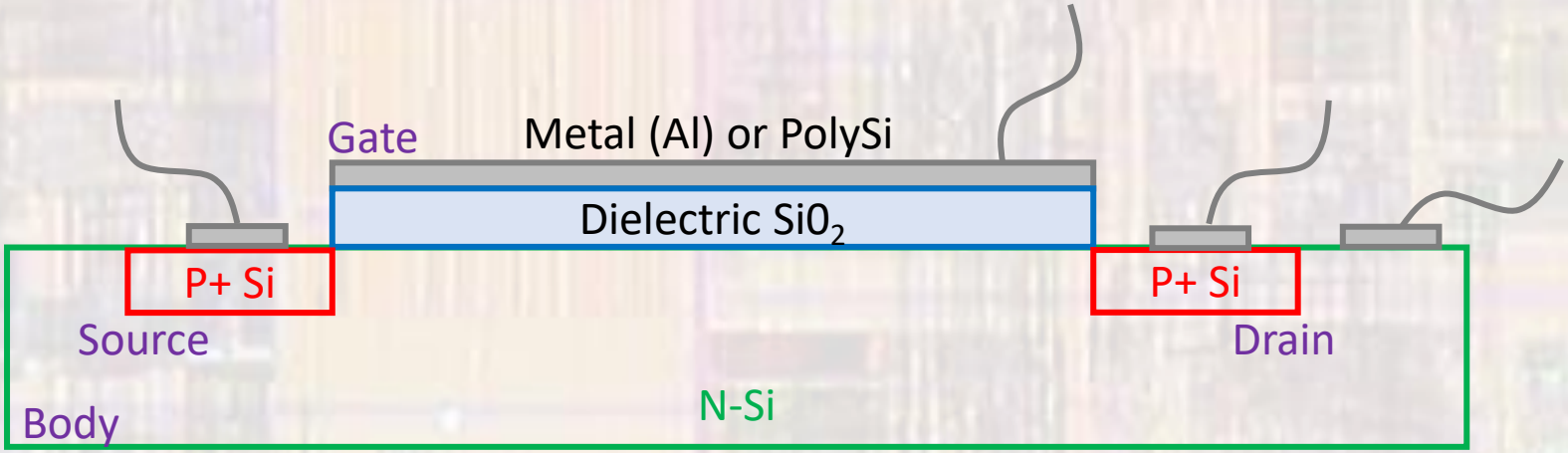


$V_{DSsat} = V_{GS} - V_{th}$

$$I_D = K_n(V_{GS} - V_{tn})^2$$

MOS I-V Characteristics

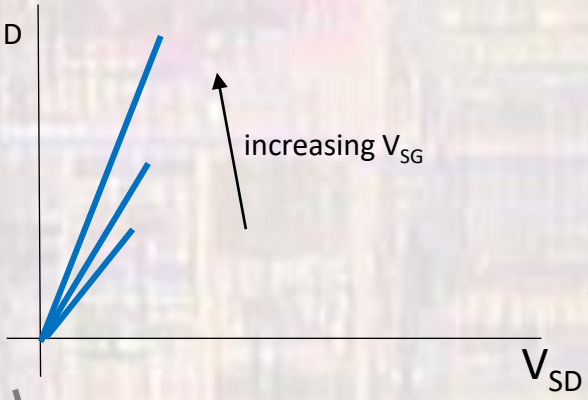
- P-MOS Operation - Cutoff
  - $V_{SG} < V_{th}$
    - No inversion region is formed
      - No holes flow from source to drain
      - No current flow from source to drain

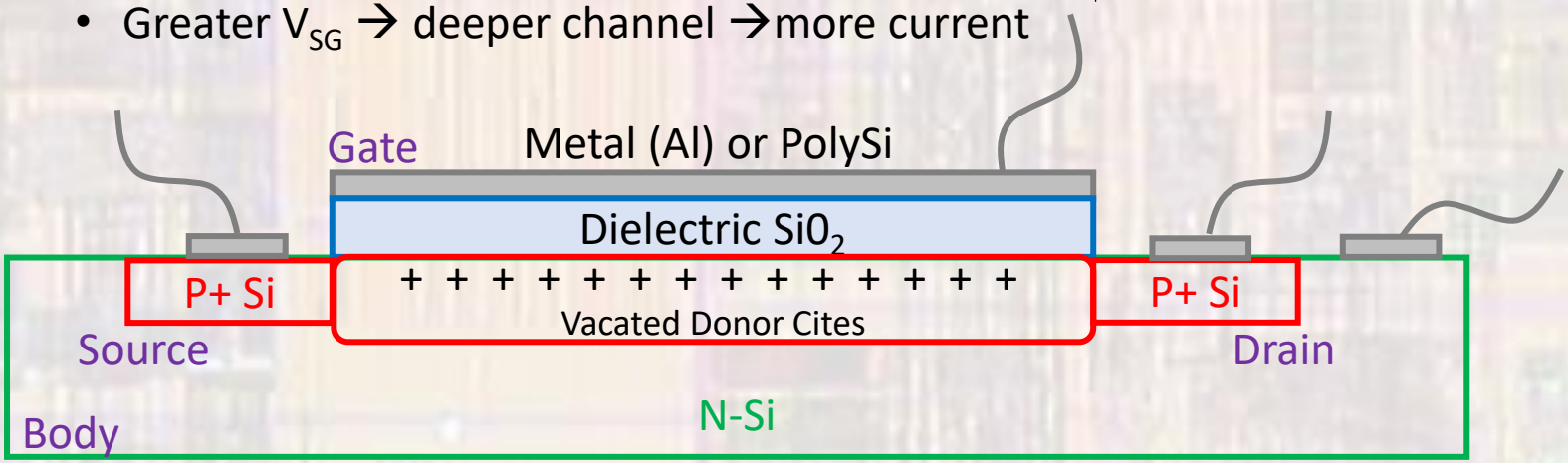


$$I_D = 0$$

MOS I-V Characteristics

- P-MOS Operation – non-saturation
  - $V_{SG} > V_{th}$
    - Inversion region is formed
      - Holes can flow from source to drain
      - Current can flow from source to drain
      - Greater V_{SG} → deeper channel →more current

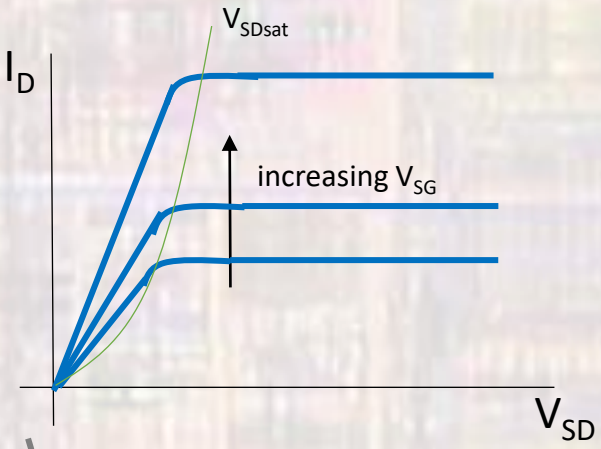


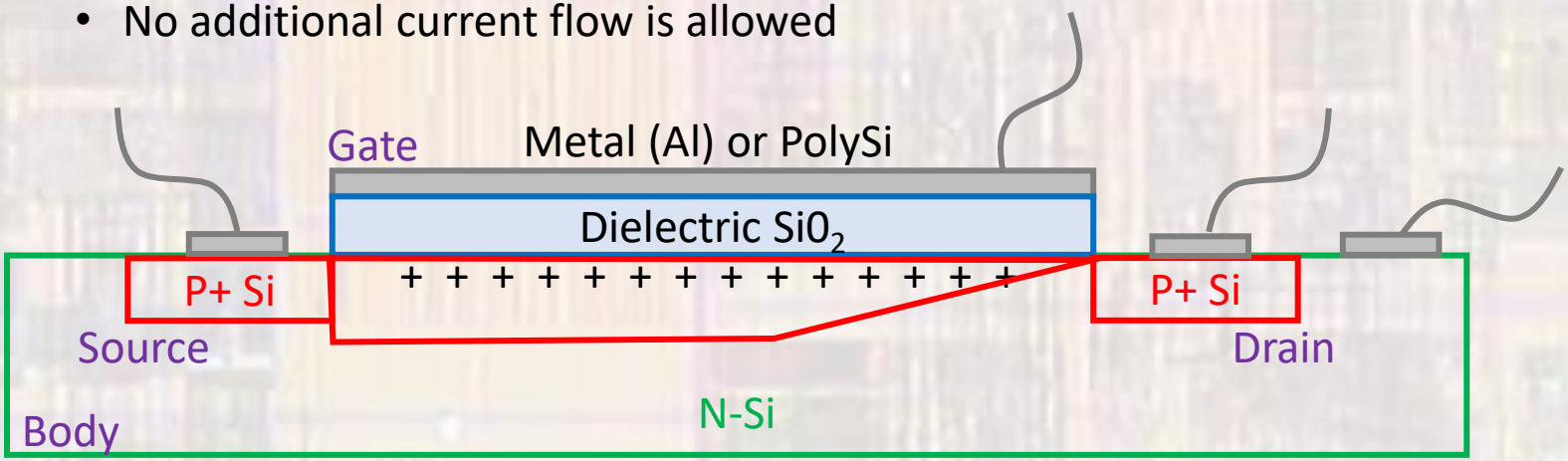


$$I_D = K_p\left[2(V_{SG} - V_{tp})V_{SD} - V_{SD}^2\right]$$

MOS I-V Characteristics

- P-MOS Operation – saturation
  - $V_{SG} > V_{th}$, $V_{SD} > V_{SDsat}$
    - Inversion region is formed
      - V_D is low enough to counteract the V_G near the drain → "pinch-off" of the channel
      - No additional current flow is allowed



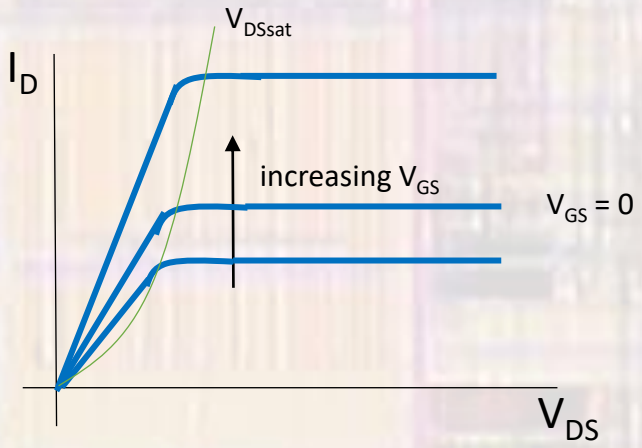


$V_{SDsat} = V_{SG} - V_{th}$

$$I_D = K_p(V_{SG} - V_{tp})^2$$

MOS I-V Characteristics

- N-MOS Depletion Mode
  - Inversion region is built into the device
    - $V_{tn} < 0$



$$I_D = K_n[2(V_{GS} - V_{tn})V_{DS} - V_{DS}^2]$$

$V_{DSsat} = V_{GS} - V_{th}$

$$I_D = K_n(V_{GS} - V_{tn})^2$$

MOS I-V Characteristics

- Parameters

$$K_n = \frac{W\mu_n C_{ox}}{2L} \qquad K_p = \frac{W\mu_p C_{ox}}{2L}$$

$$K_n = \frac{k'_n}{2}\frac{W}{L} \qquad K_p = \frac{k'_p}{2}\frac{W}{L}$$

$$k'_n = \mu_n C_{ox} \qquad k'_p = \mu_p C_{ox}$$

μ_n, μ_n, C_{ox} fixed for a given semiconductor process →

k'_n, k'_p fixed for a given semiconductor process

$$I_D = K_n[2(V_{GS} - V_{tn})V_{DS} - V_{DS}^2] \qquad I_D = K_p[2(V_{SG} - V_{tp})V_{SD} - V_{SD}^2]$$

$$I_D = \frac{k'_n}{2}\frac{W}{L}[2(V_{GS} - V_{tn})V_{DS} - V_{DS}^2] \qquad I_D = \frac{k'_p}{2}\frac{W}{L}[2(V_{SG} - V_{tp})V_{SD} - V_{SD}^2]$$

$V_{DSsat} = V_{GS} - V_{th}$ $\qquad$ $V_{SDsat} = V_{SG} - V_{th}$

$$I_D = K_n(V_{GS} - V_{tn})^2 \qquad I_D = K_p(V_{SG} - V_{tp})^2$$

$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_{tn})^2 \qquad I_D = \frac{k'_p}{2}\frac{W}{L}(V_{SG} - V_{tp})^2$$

MOS Gate Capacitance

- Parameters
  - W – Transistor Width
  - L – Transistor length (channel length)
  - t_{ox} – thickness of the oxide
    - 15-20 Angstroms – 3 to 4 atom layers
    - $1.5 – 2.0 \times 10^{-9}$ m
  - ε_0 – permittivity (dielectric constant) of free space
    - 8.85×10^{-12} F/m
  - $\varepsilon_r(SiO_2)$ – relative permittivity multiplier for SiO_2
    - 3.9

$$C_G = W \times L \times C_{ox} = W \times L \times {\varepsilon_{ox}}/{t_{ox}} = W \times L \times {\varepsilon_0 \varepsilon_r}/{t_{ox}}$$

$$C_{Gn} = W \times L \times {k'_n}/{\mu_n} \qquad C_{Gp} = W \times L \times {k'_p}/{\mu_p}$$