N-MOS Circuits

Last updated 4/5/22

N-MOS Circuits

- Parameters $K_n = \frac{W \mu_n C_{ox}}{2L}$

$$K_n = \frac{k'_n}{2}\frac{W}{L} \qquad k'_n = \mu_n C_{ox}$$

μ_n, C_{ox} fixed for a given semiconductor process →

k'_n fixed for a given semiconductor process

$$I_D = K_n[2(V_{GS} - V_{tn})V_{DS} - V_{DS}^2]$$

$$I_D = \frac{k'_n}{2}\frac{W}{L}[2(V_{GS} - V_{tn})V_{DS} - V_{DS}^2]$$

$$C_{Gn} = W \times L \times {k'_n}/{\mu_n}$$

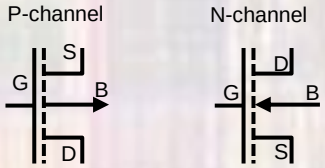
$V_{DSsat} = V_{GS} - V_{th}$

$$I_D = K_n(V_{GS} - V_{tn})^2$$

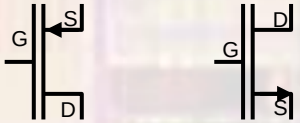
$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_{tn})^2$$

N-MOS Circuits

- Enhancement Mode
  - A bias is required to form the channel
  - 4-terminal symbol



  - In digital applications the Source is typically tied to
    - Vdd for P-MOS
    - Gnd for N-MOS

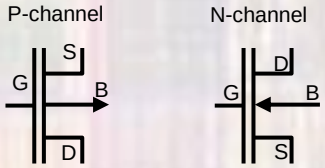


  - The simplified logic symbols

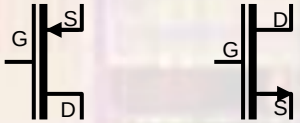
Note – almost all N-MOS and P-MOS devices used today are enhancement mode – so the dashed line is omitted

N-MOS Circuits

- Depletion Mode
  - No bias is required to form the channel
  - 4-terminal symbol



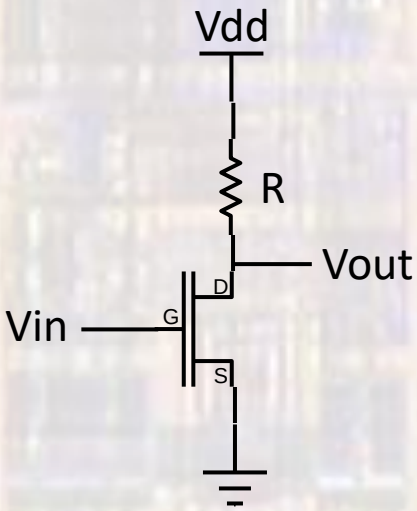
  - In digital applications the Source is typically tied to
    - Vdd for P-MOS
    - Gnd for N-MOS



  - The simplified logic symbols

N-MOS Circuits

- Simple Inverter - Design



Assuming Vdd is big enough to keep the NMOS device in saturation at the switching point

$$\frac{V_{dd} - V_{ds}}{R} = \frac{k'_n}{2}\frac{W}{L}(V_{ds} - V_t)^2$$

Desire a switching point mid way

$$V_{out} = V_{in} = {}^{V_{dd}}/_{2} = {}^{V_{ds}}/_{2}$$

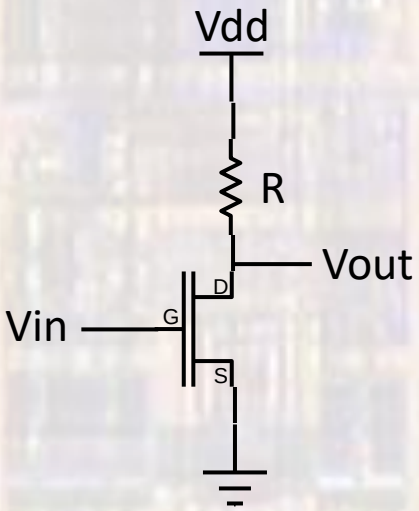
$$\frac{{}^{V_{dd}}/_{2}}{R} = \frac{k'_n}{2}\frac{W}{L}\left({}^{V_{dd}}/_{2} - V_t\right)^2$$

$$R = \frac{{}^{V_{dd}}/_{2}}{\frac{k'_n}{2}\frac{W}{L}\left({}^{V_{dd}}/_{2} - V_t\right)^2}$$

$$\frac{W}{L} = \frac{{}^{V_{dd}}/_{2}}{R\frac{k'_n}{2}\left({}^{V_{dd}}/_{2} - V_t\right)^2}$$

N-MOS Circuits

- Simple Inverter - Design



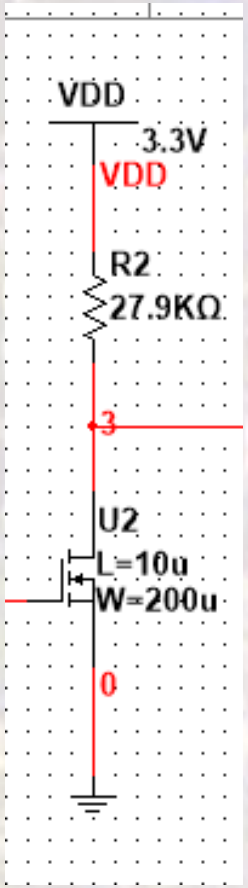
Vt = 1V
Vdd = 3.3V
W/L = 20
k'n = 14uA/V²

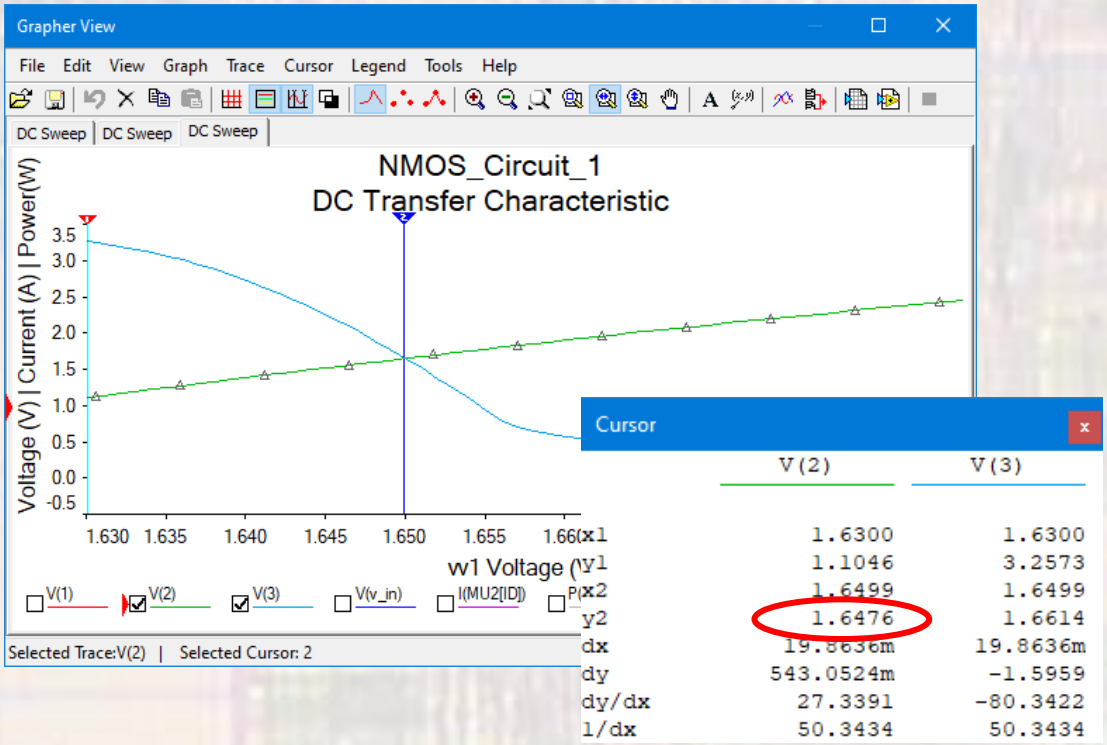
$$R = \frac{V_{dd}/2}{\frac{k'_n}{2}\frac{W}{L}\left(V_{dd}/2 - V_t\right)^2}$$

$$R = 27.9K\Omega$$

N-MOS Circuits

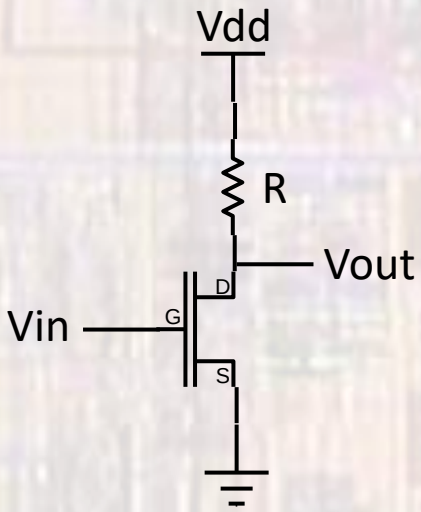
- Simple Inverter - Design

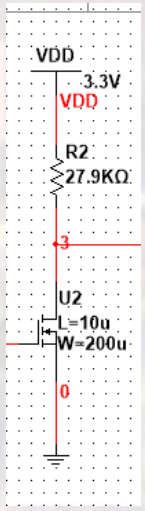




N-MOS Circuits

- Simple Inverter – Design
  - Power dissipation
    - Vin low – 0mA
    - Vin High – (Vdd/R)
    - P_{ave} = (Vdd/2R)xVdd

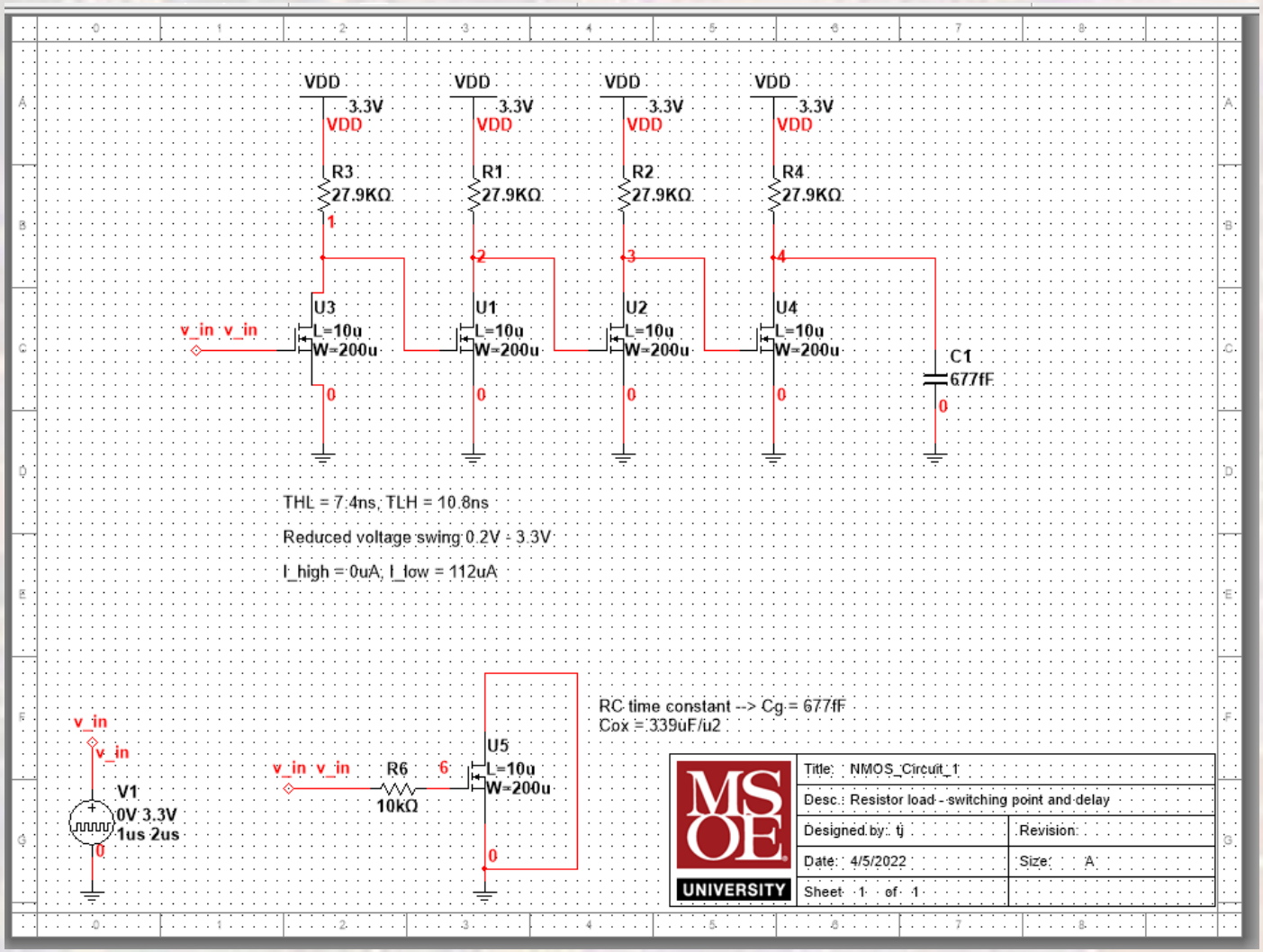




Pave = (3.3V/55.8KΩ)x3.3V = 195uW

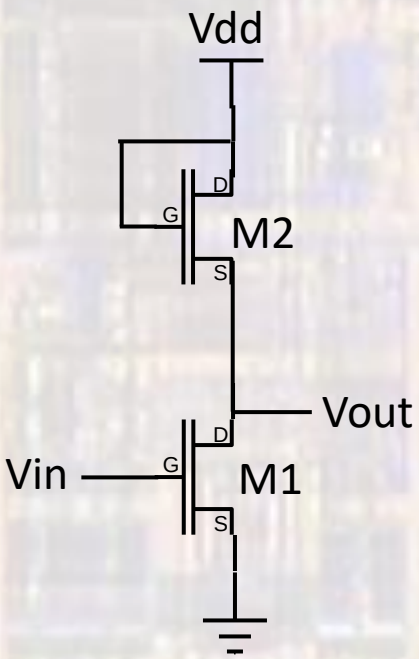
N-MOS Circuits

- Simple Inverter – Design



N-MOS Circuits

- Enhancement Load Inverter - Design



M2 is always in saturation

For Vin = 0, Id1 = Id2 = 0

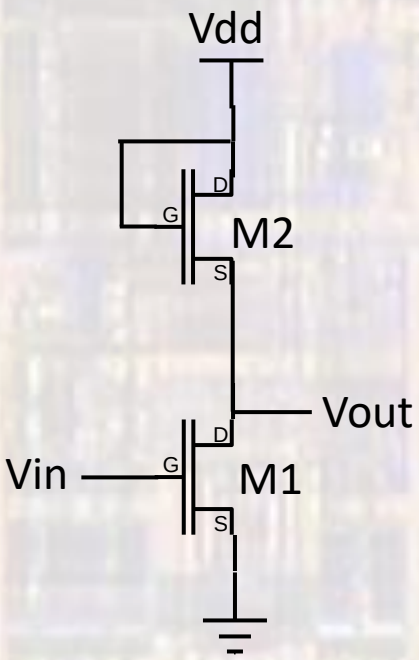
$$I_{d2} = \frac{k'_n}{2}\frac{W2}{L2}\left(V_{gs2} - V_t\right)^2 = 0$$

→ $V_{gs2} = V_t = V_{ds2}$

Maximum $V_{OH} = V_{dd} - V_t$

N-MOS Circuits

- Enhancement Load Inverter - Design



M2 is always in saturation
Assuming Vdd is big enough to keep M1 in saturation at the switching point

$$\frac{k'_n}{2}\frac{W2}{L2}\left(V_{gs2}-V_t\right)^2=\frac{k'_n}{2}\frac{W1}{L1}\left(V_{gs1}-V_t\right)^2$$

$$\frac{k'_n}{2}\frac{W2}{L2}\left(V_{dd}-V_{out}-V_t\right)^2=\frac{k'_n}{2}\frac{W1}{L1}\left(V_{in}-V_t\right)^2$$

Desire a consistent switching point Vin = Vout

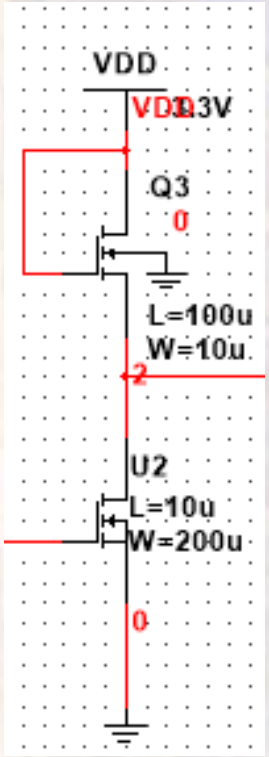
$$V_{switch}=\frac{V_{dd}-V_t+V_t\left(1+\sqrt{\frac{W1/L1}{W2/L2}}\right)}{1+\sqrt{\frac{W1/L1}{W2/L2}}}$$

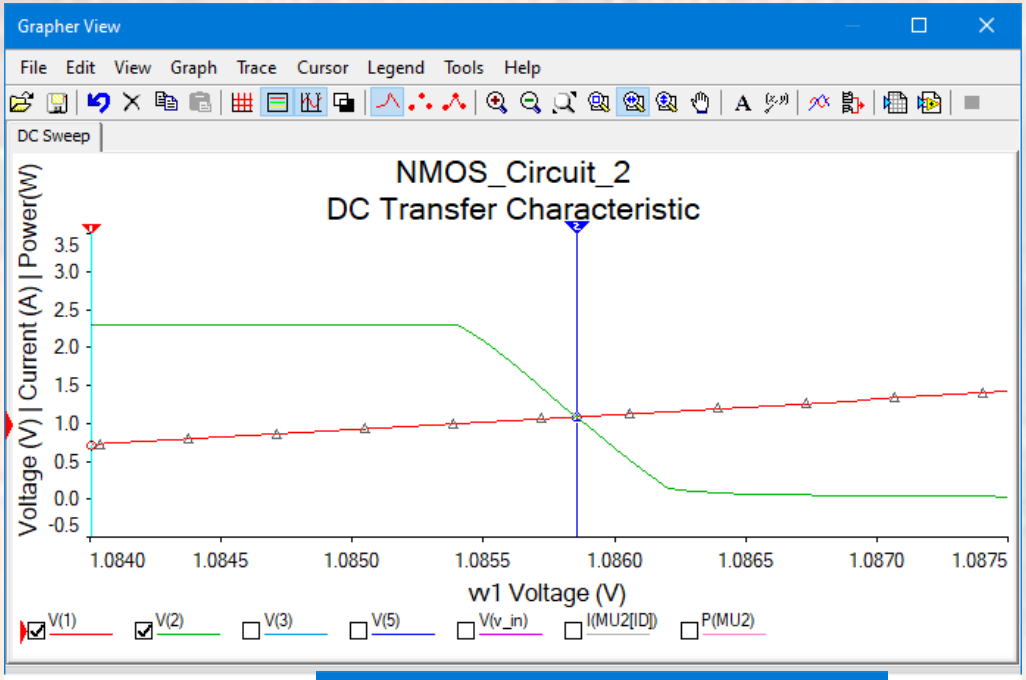
$$\frac{W1/L1}{W2/L2}=\left(\frac{V_{dd}-V_t}{V_{sw}-V_t}-1\right)^2$$

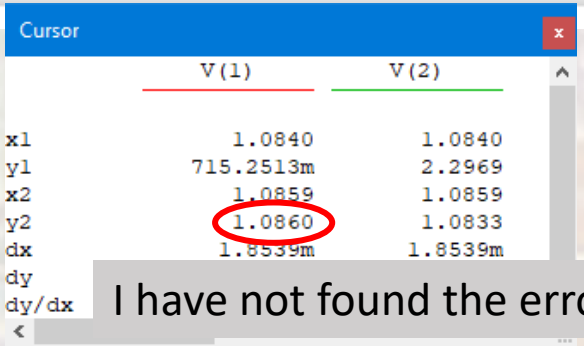
N-MOS Circuits

- Enhancement Load Inverter - Design

Vt = 1V
Vdd = 3.3V
k'n = 14uA/V^2





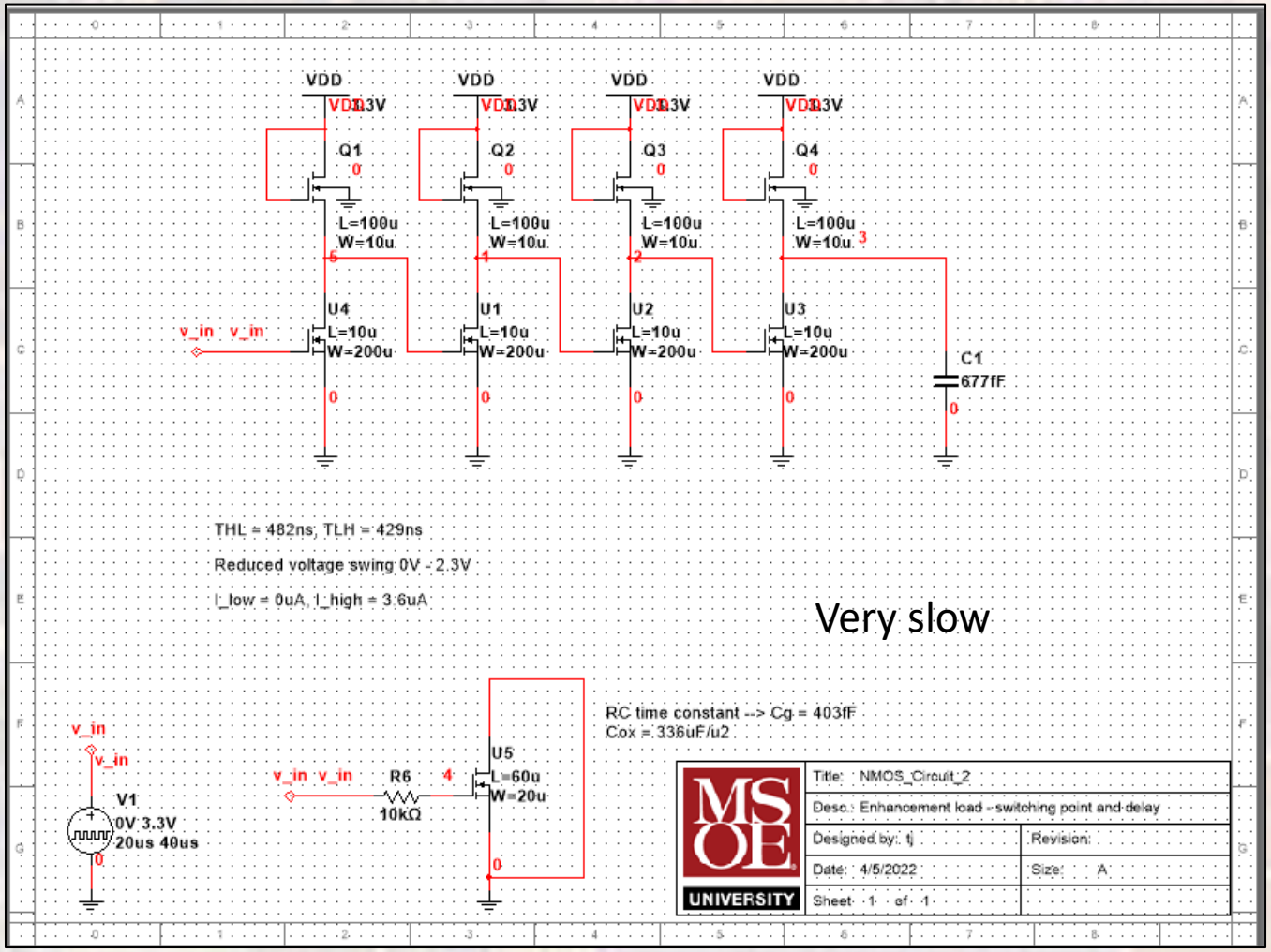


1.15V switching pt
→ 200:1 W/L ratio

I have not found the error here

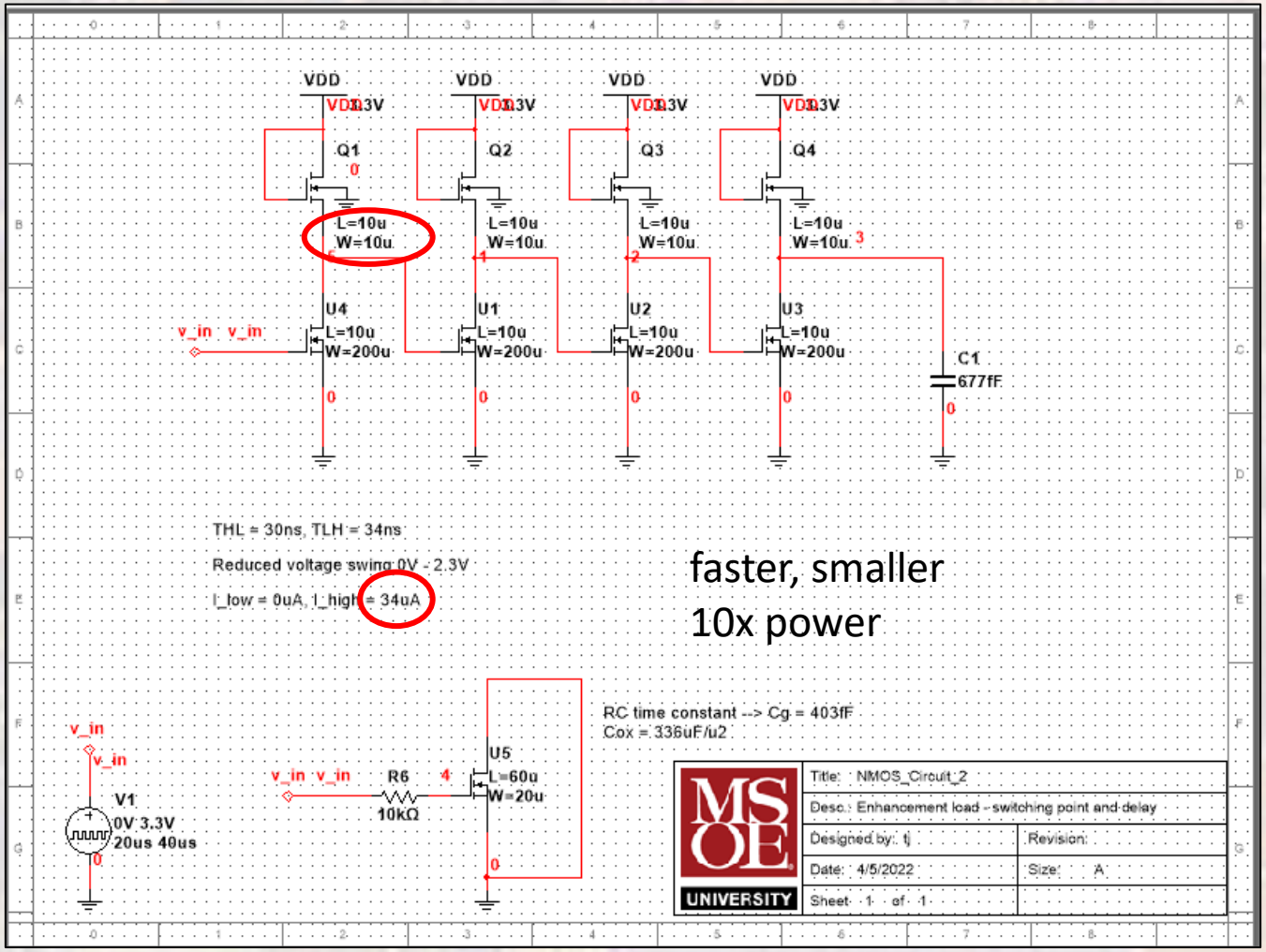
N-MOS Circuits

- Enhancement Load Inverter - Design



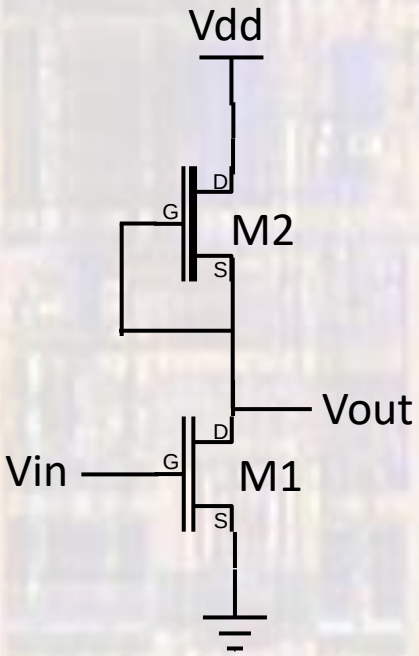
N-MOS Circuits

- Enhancement Load Inverter - Design



N-MOS Circuits

- Depletion Load Inverter - Design



M2 Vgs = 0

Assuming Vdd is big enough to keep M2 and M1 in saturation at the switching point

$$\frac{k'_{nd}}{2}\frac{W2}{L2}\left(V_{gs2}-V_{td}\right)^2=\frac{k'_{n}}{2}\frac{W1}{L1}\left(V_{gs1}-V_t\right)^2$$

$$\frac{k'_{nd}}{2}\frac{W2}{L2}\left(-V_{td}\right)^2=\frac{k'_{n}}{2}\frac{W1}{L1}\left(V_{gs1}-V_t\right)^2$$

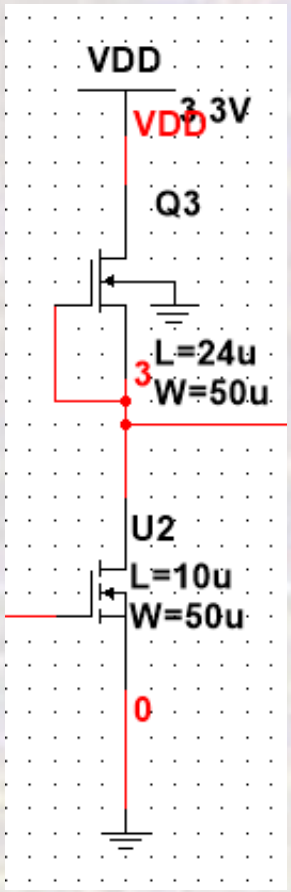
Desire a consistent switching point Vin = Vout

$$\frac{k'_{nd}}{2}\frac{W2}{L2}\left(-V_{td}\right)^2=\frac{k'_{n}}{2}\frac{W1}{L1}\left(Vdd/2-V_t\right)^2$$

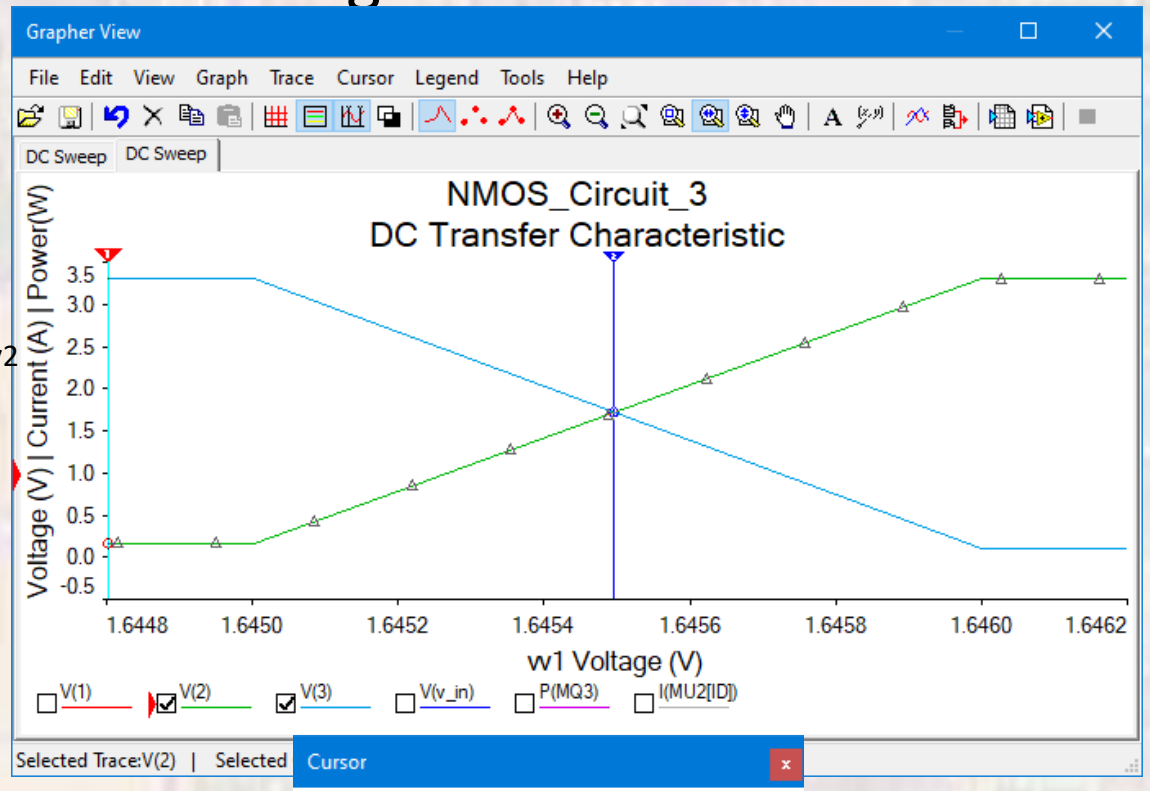
$$\frac{W1/L1}{W2/L2}=\left(\frac{-V_{td}}{\left(V_{dd}/2-V_t\right)}\right)^2$$

N-MOS Circuits

- Depletion Load Inverter - Design

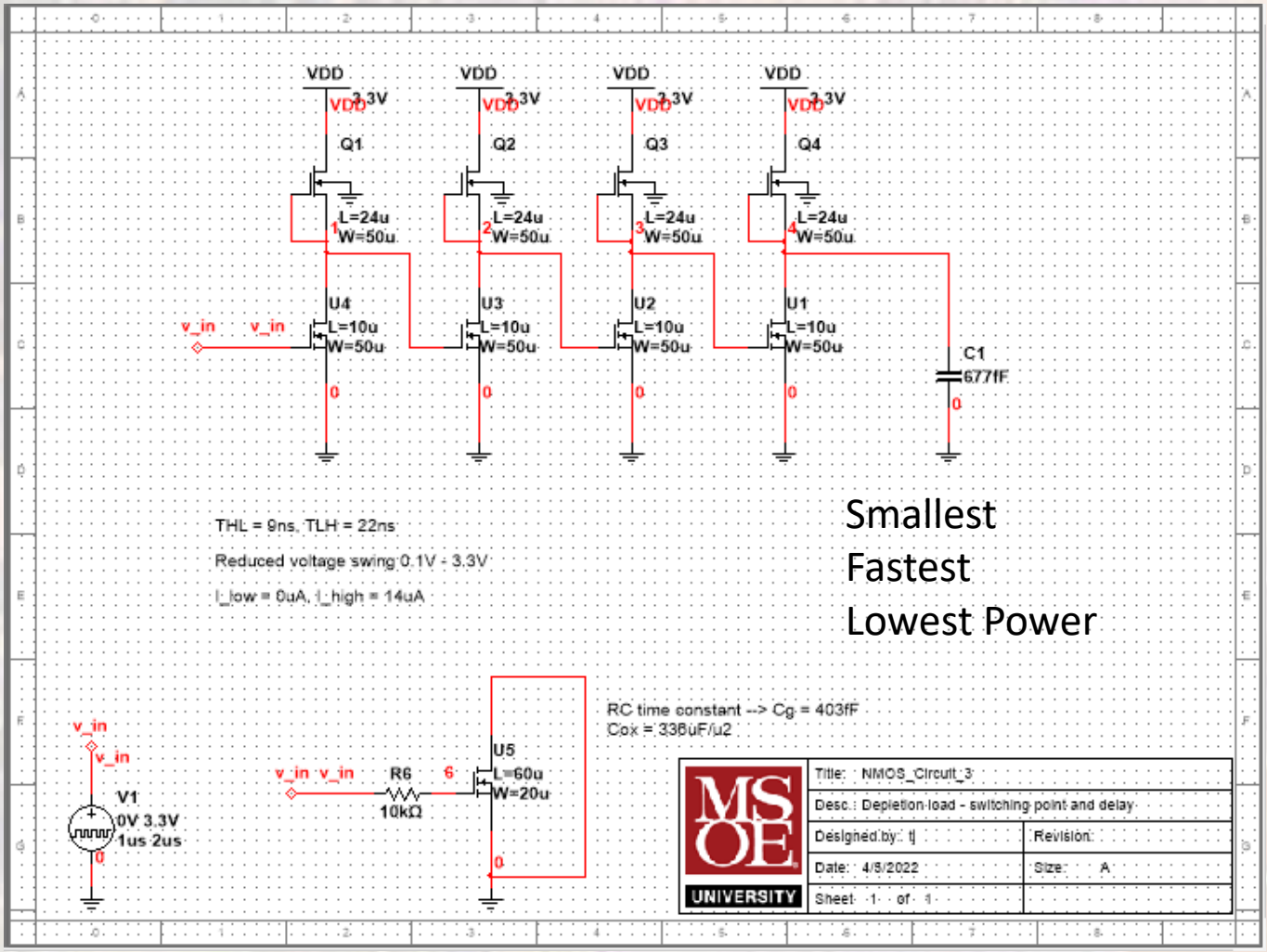


Vt = 1V
Vtd = -1V
Vdd = 3.3V
k'n = 14uA/V^2
k'nd = 14uA/V^2



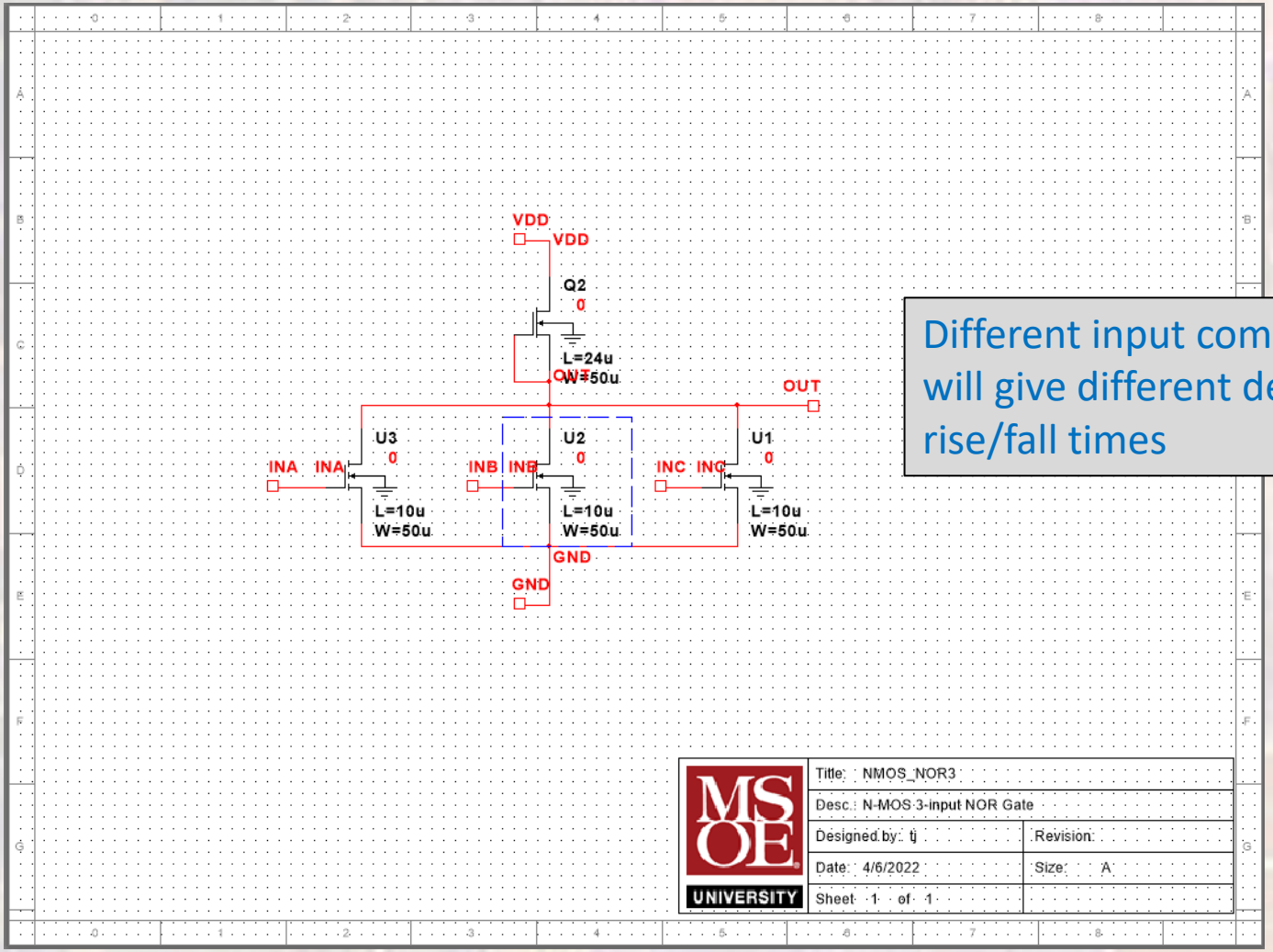
N-MOS Circuits

- Depletion Load Inverter - Design



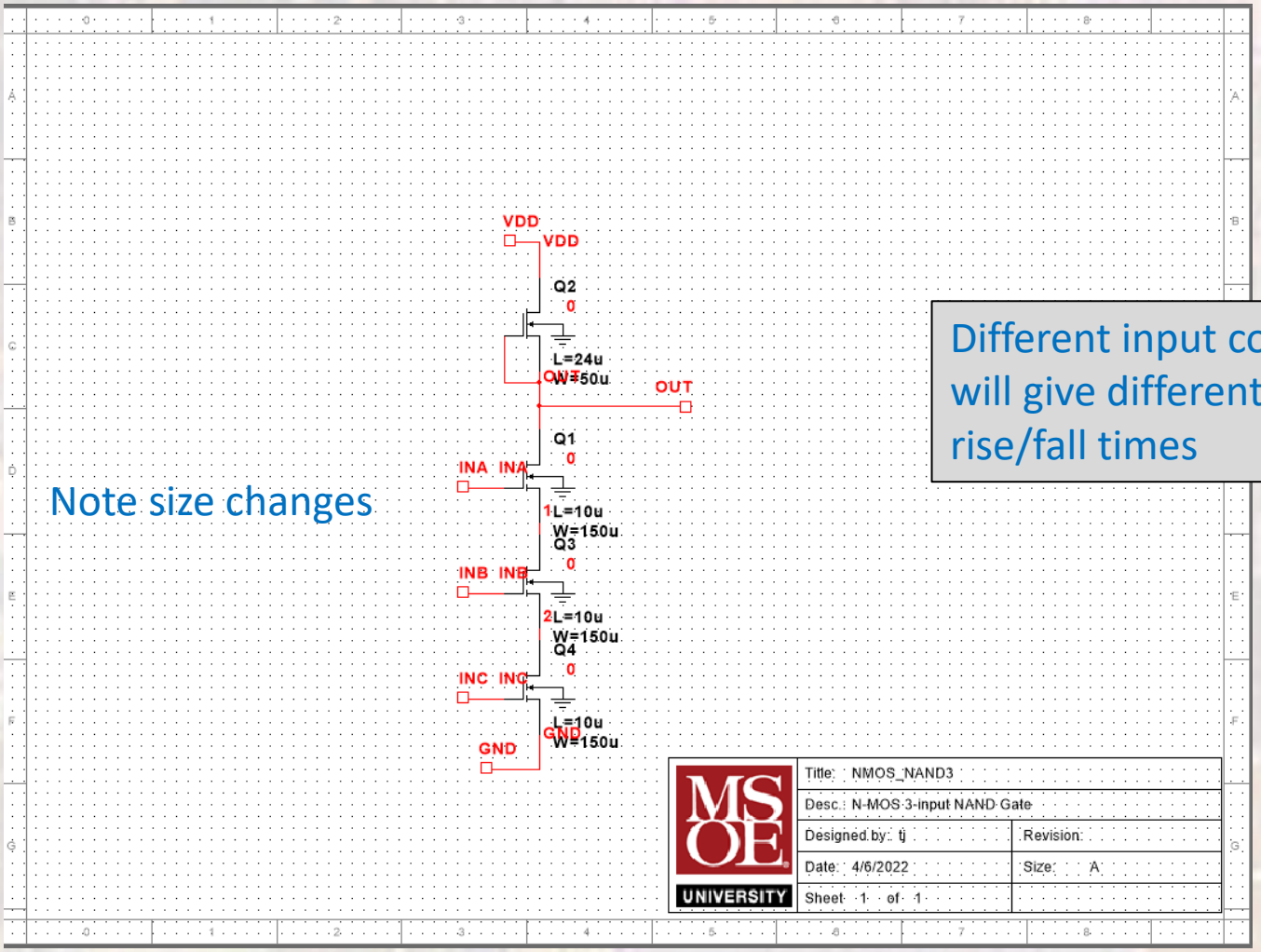
N-MOS Circuits

- N-MOS Gates



N-MOS Circuits

- N-MOS Gates



N-MOS Circuits

- N-MOS Gates