CMOS Logic Area

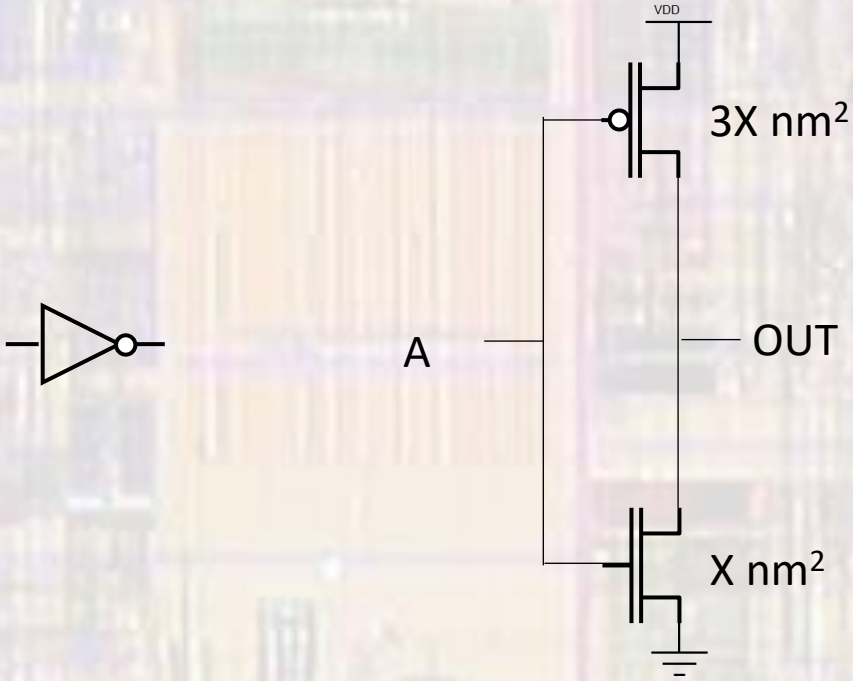
Last updated 1/6/25

CMOS Logic Area

- Device area is the key driver for logic area calculations
  - Minimum device lengths and widths set minimum device area
  - In most technologies, P-MOS devices have approximately 1/3 the strength of N-MOS device
    - To keep gates balanced, P-MOS devices need to be 3x as large as N-MOS devices
  - Devices in series must be made larger due to the need to make the series path through multiple devices the same strength as a single device

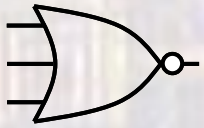
CMOS Logic Area

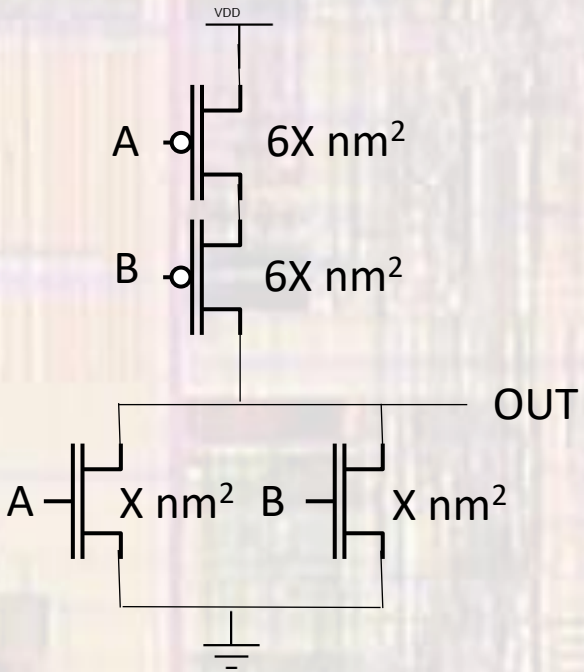
- CMOS Gates – INV
  - Total area: 4X nm^2



CMOS Logic Area

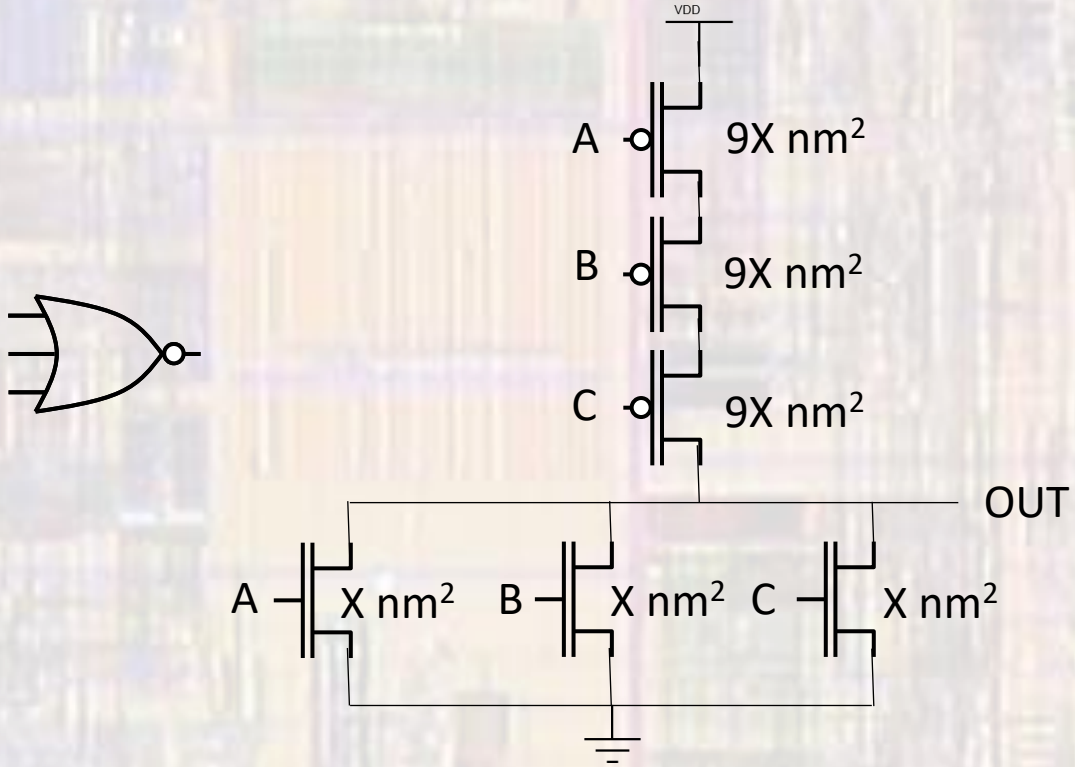
- CMOS Gates – NOR_2
  - Total area: 14X nm^2





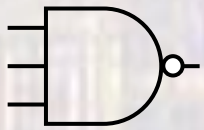
CMOS Logic Area

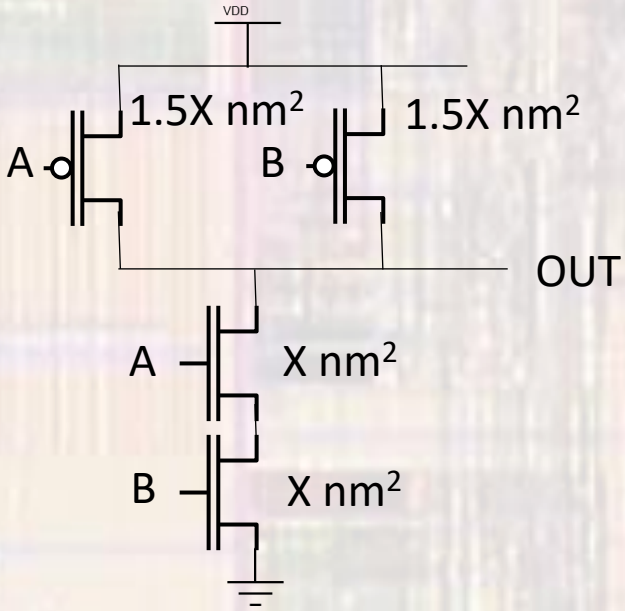
- CMOS Gates – NOR_3
  - Total area: 30X nm^2



CMOS Logic Area

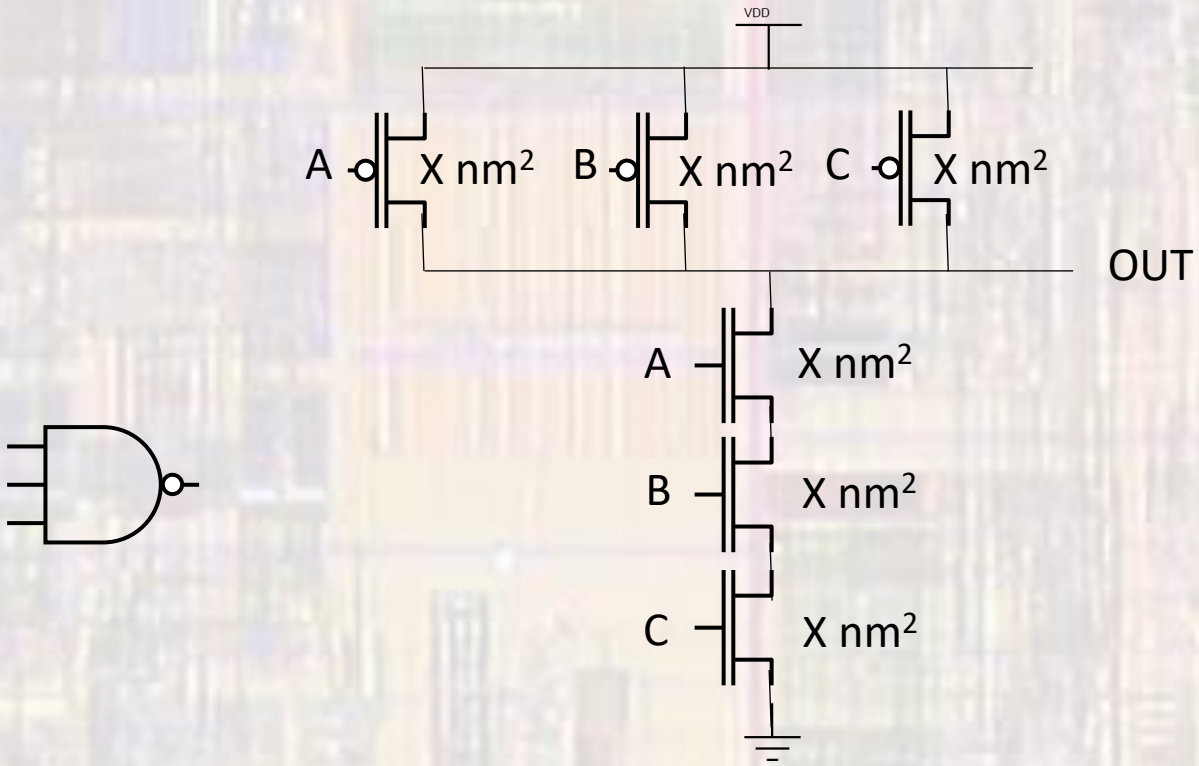
- CMOS Gates – NAND_2
  - Total area: 5X nm^2





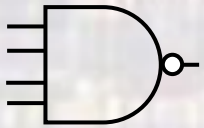
CMOS Logic Area

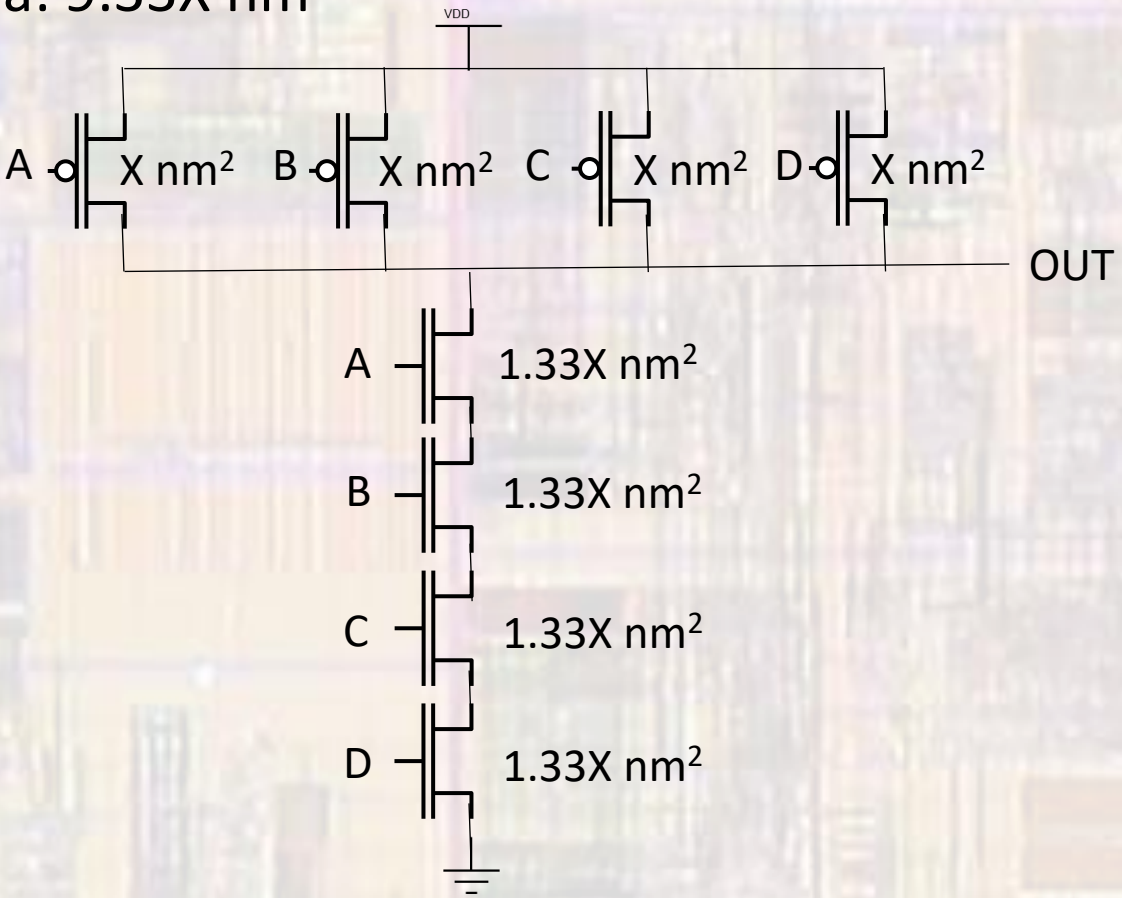
- CMOS Gates – NAND_3
  - Total area: 6X nm^2



CMOS Logic Area

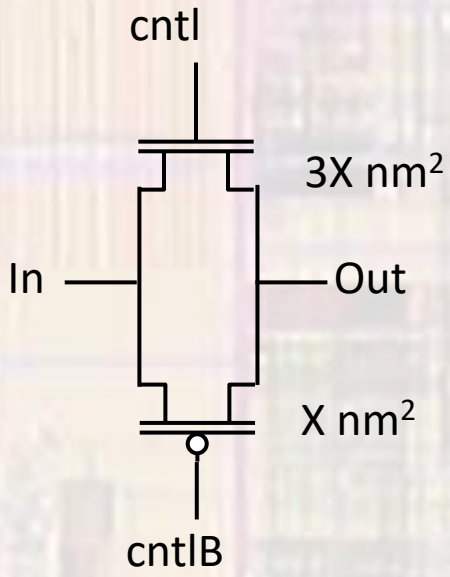
- CMOS Gates – NAND_4
  - Total area: 9.33X nm^2





CMOS Logic Area

- CMOS Transmission Gates
  - Total area: 4X nm^2
  - Often we just make them the same size → 2X nm^2



CMOS Logic Area

- Summary
  - NAND gates preferred over NOR gates

Gate	Area (X nm^2)
INV	4
NOR_2	14
NOR_3	30
NAND_2	5
NAND_3	6
NAND_4	9.33
T-Gate	4