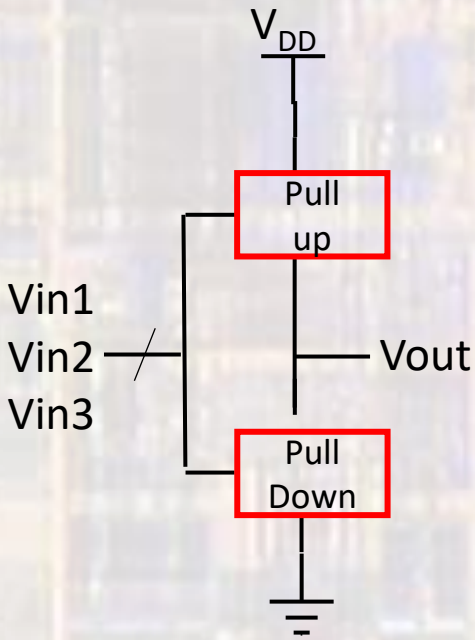
CMOS Logic Circuits

Last updated 10/31/24

CMOS Logic Circuits

- Gate Concepts



We can generalize our inverter results to account for more complex gates

Ensure every input combination results in either:

The Pull-up network provides a path to V_{DD}

or

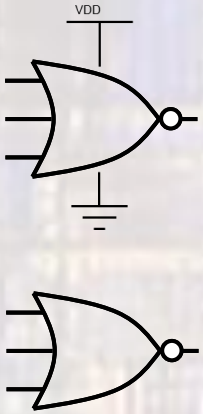
The Pull-down network provides a path to GND

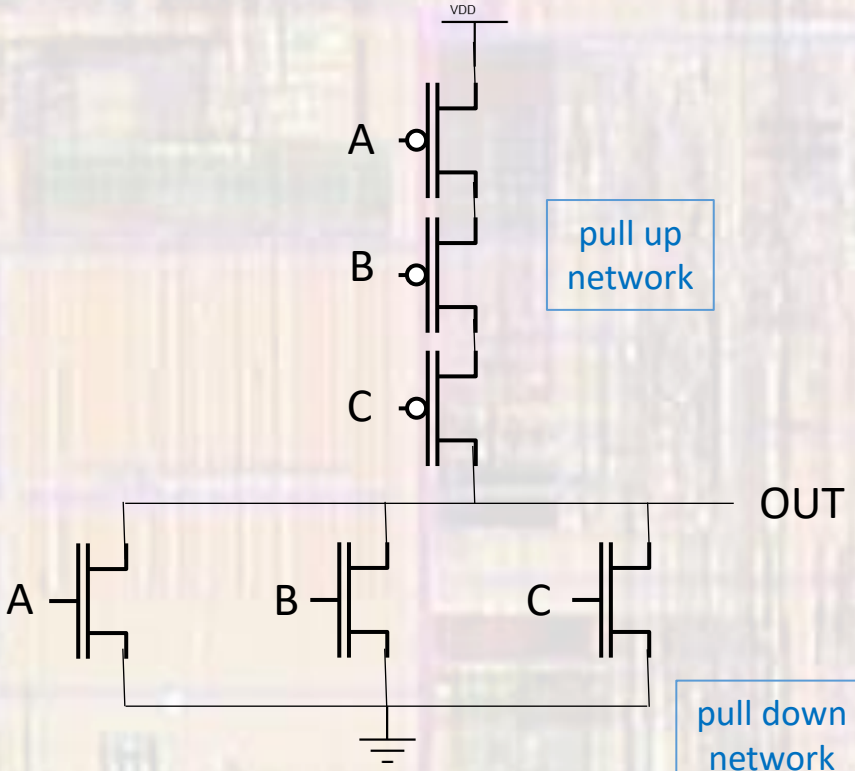
never

Both

CMOS Logic Circuits

- CMOS Gates - NOR



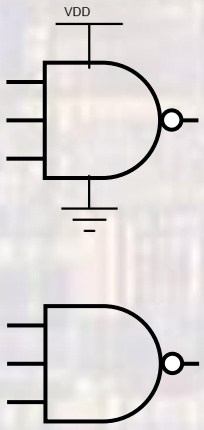


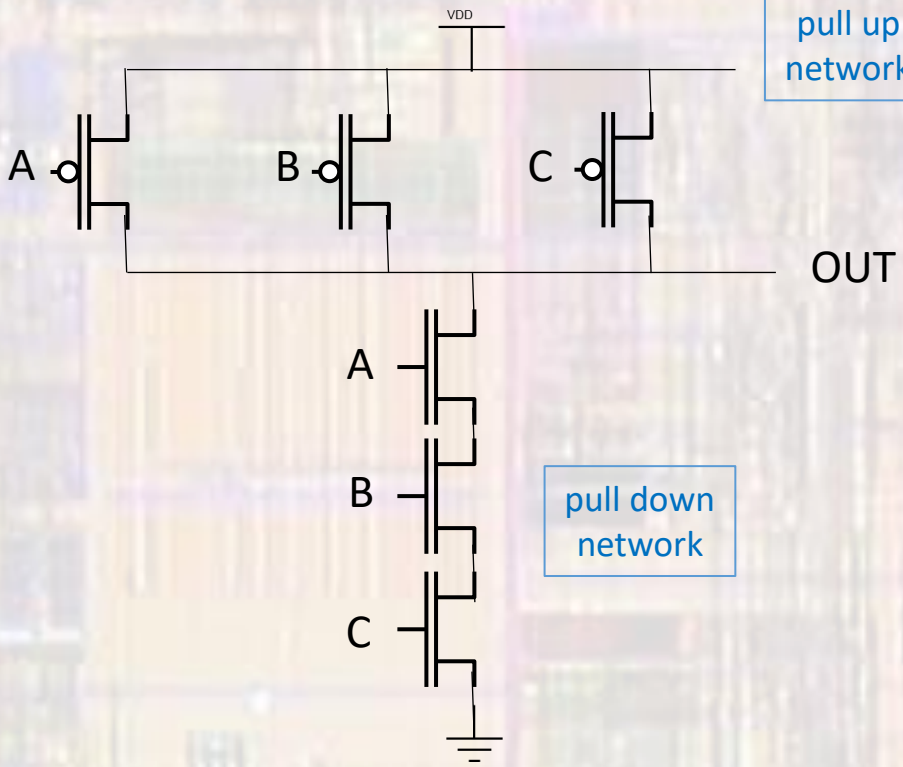
A	B	C	NOR OUT
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

If ANY input is high, pull-down is on, pull-up is off → output is low
If ALL inputs are low, pull-down is off, pull-up is on → output is high

CMOS Logic Circuits

- CMOS Gates - NAND





A	B	C	NAND OUT
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

If ANY input is low, pull-up is on, pull-down is off → output is high
If ALL inputs are high, pull-up is off, pull-down is on → output is low

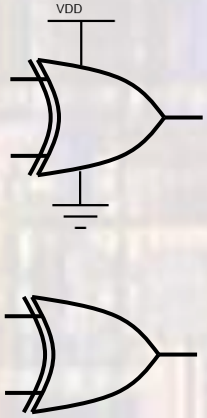
CMOS Logic Circuits

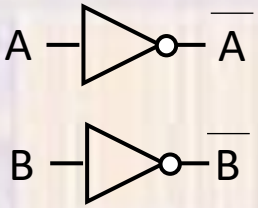
- AND / OR
  - Note – CMOS technology has an inherent inversion operation when configured into a gate
  - AND gates require a NAND gate and an Inverter

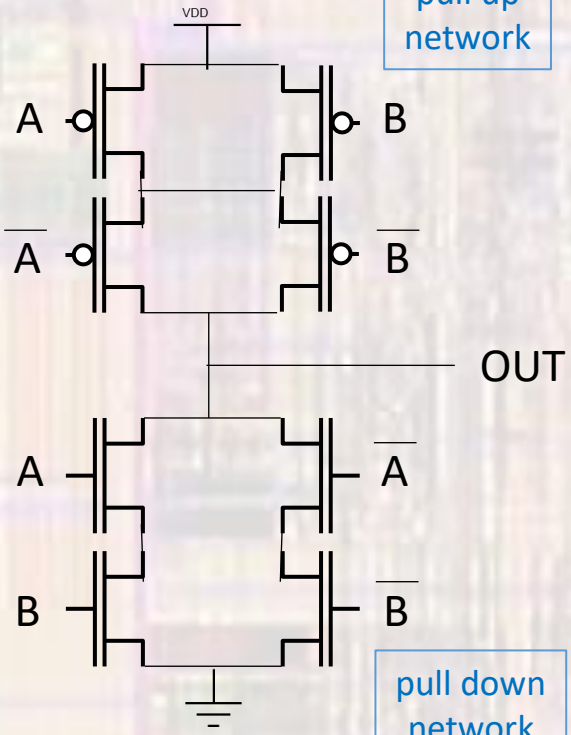
  - OR gates require a NOR gate and an Inverter

CMOS Logic Circuits

- XOR





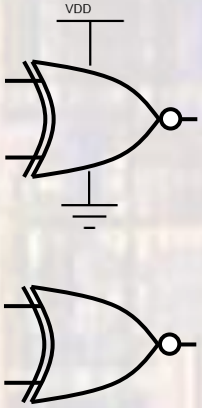


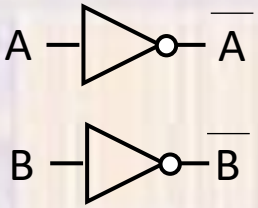
A	B	A ⊗ B
1	1	0
1	0	1
0	1	1
0	0	0

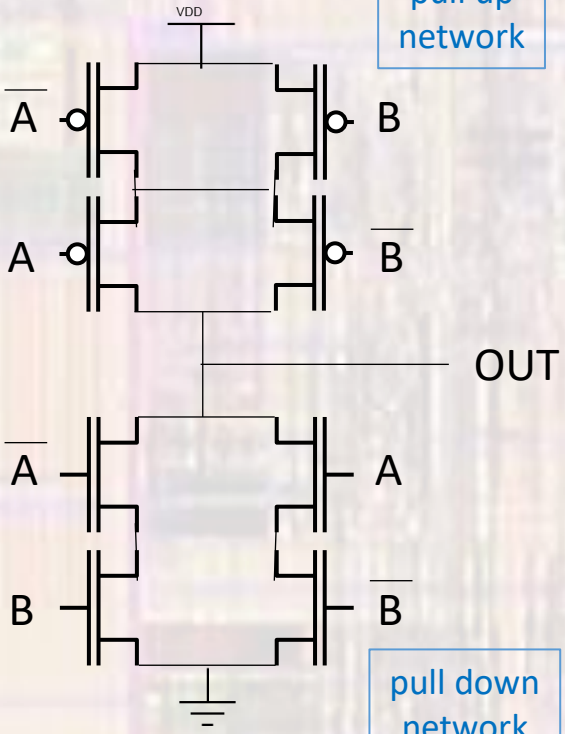
If ONLY ONE input is high, pull-up is on, pull-down is off → output is high

CMOS Logic Circuits

- XNOR





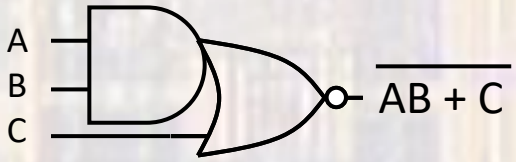


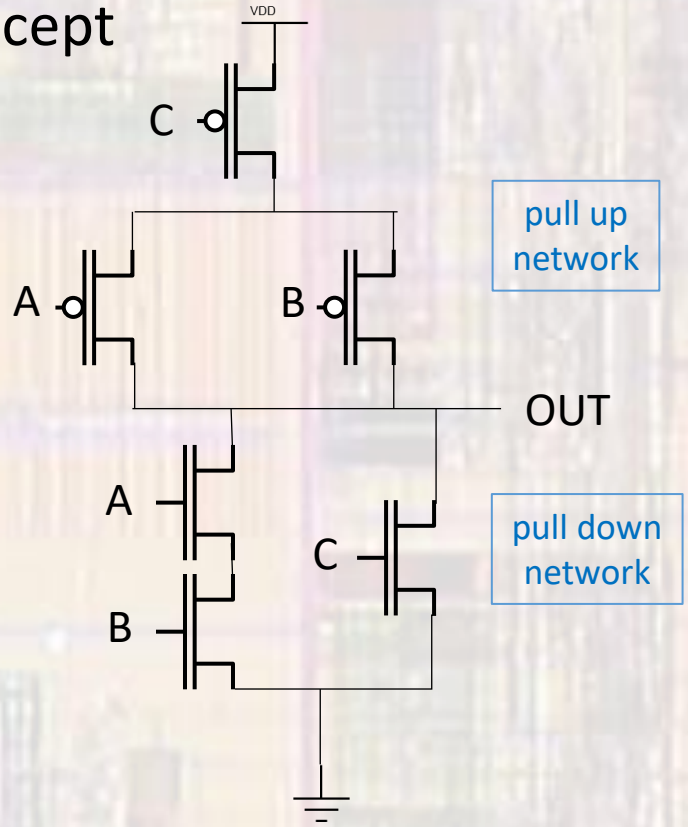
A	B	A ⊙ B
1	1	1
1	0	0
0	1	0
0	0	1

If ONLY ONE input is high, pull-down is on, pull-up is off → output is low

CMOS Logic Circuits

- Complex Gates
  - Special function gates can be created using the Pull-up / Pull-down concept

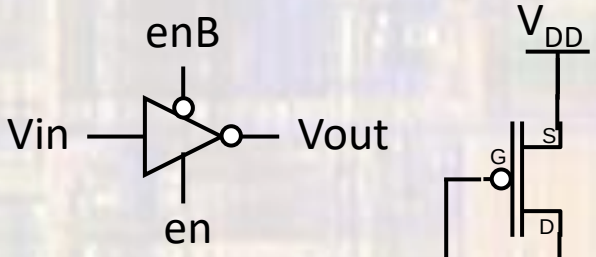




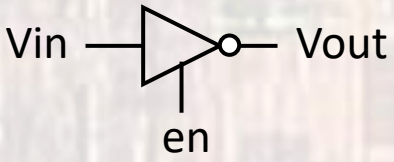
A	B	C	$\overline{AB + C}$
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

CMOS Logic Circuits

- CMOS Tristate Inverter
  - What can we do if we want multiple circuits to drive a single wire (but never at the same time)



en	in	OUT
0	0	Open ckt
0	1	Open ckt
1	0	! In (1)
1	1	! In (0)



en = 0 → Vout = open ckt

en = 1 → Vout = ! Vin

CMOS Logic Circuits

- CMOS Transmission Gates
  - Use parallel P-MOS and N-MOS devices as a “pass gate”
    - Passes both ‘0’s and ‘1’s
    - Bi-directional
    - Requires cntl and cntlB