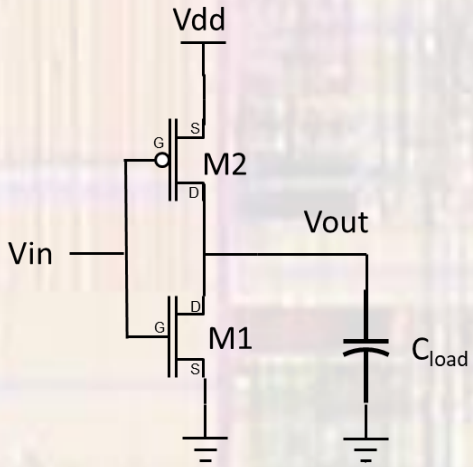
CMOS Logic Power

Last updated 10/29/24

CMOS Logic Power

- 3 Major power components
  - DC power
  - Switching power
  - Shoot-Through power

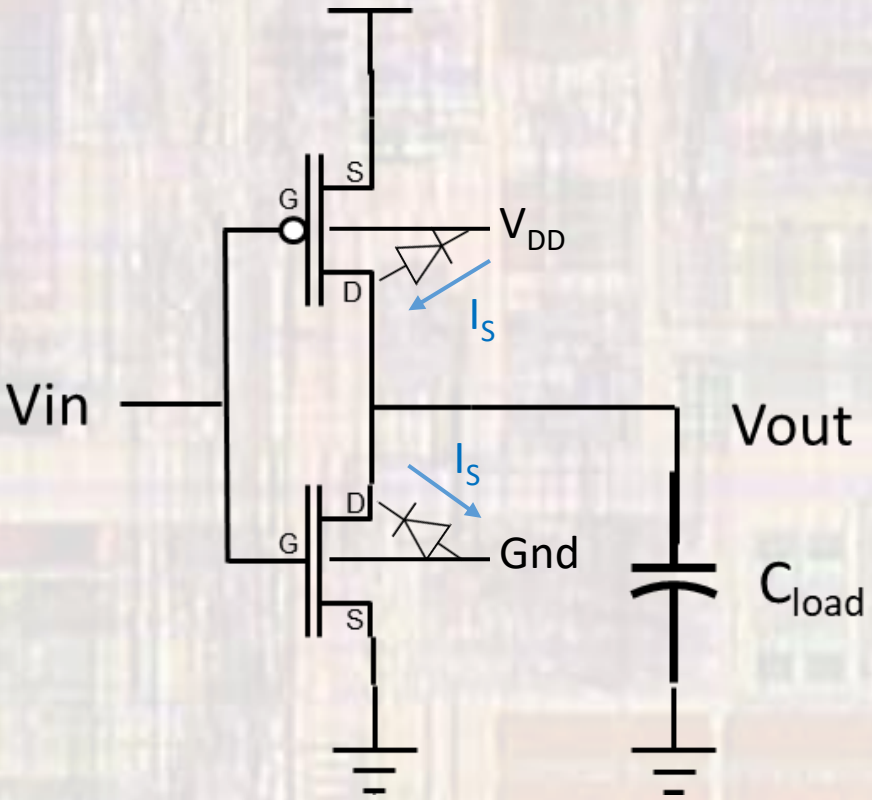


CMOS Logic Power

- DC power
  - Junction leakage (Drain to Body)
    - Reverse diode leakage
      - Vout = 0 P-channel leaks
      - Vout = V_{DD} N-channel leaks
    - Small for each device
      - Typically, $1x10^{-12}$ A / device
      - Can add up with 100M devices

Power $\cong I_S \times V_{DD}$

Power is proportional to V_{DD}

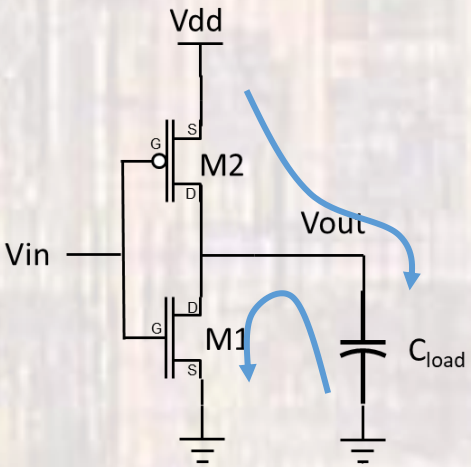


CMOS Logic Power

- Switching Power
  - Charging / Dis-charging the load and parasitic Cs
    - Load is the gate(s) driven by the output
  - Worst case
    - Rise and fall with every change (Frequency – F)

$$P = C_{load} V_{DD}^2 F$$

Power is proportional to V_{DD}^2

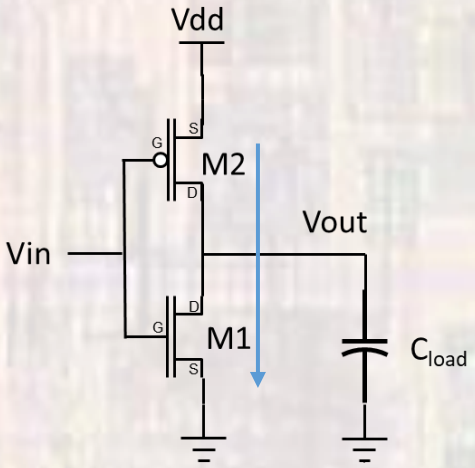


CMOS Logic Power

- Shoot-Through
  - Short period of time when both devices are on
  - Current from V_{DD} to Gnd
    - Can be large but for very short periods of time

$$P = I_{peak} V_{dd} \left(\frac{t_r + t_f}{2} \right) F$$

Power is proportional to V_{DD}

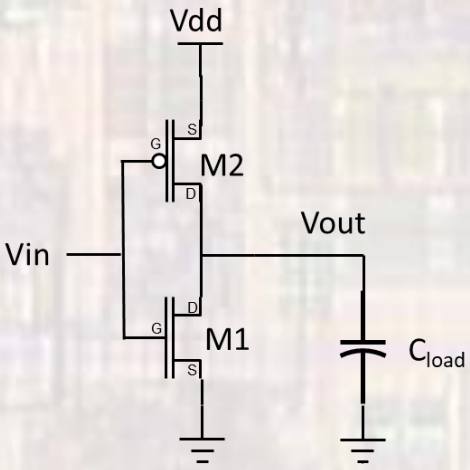


CMOS Logic Power

- Total power
  - α – proportion of clock intervals switching
  - β – leakage factor (number of gates * leakage current)

$$P = P_{DC} + P_{SW} + P_{Shoot}$$

$$P = \beta V_{DD} + \alpha C_{load} V_{DD}^2 F + \alpha I_{peak} V_{DD} \left(\frac{t_r + t_f}{2}\right) F$$



All terms are a function of V_{DD}

Operate at the lowest possible V_{DD}