

CMOS Timing Characteristics

Last updated 10/24/24

These slides introduce the basics of a CMOS timing

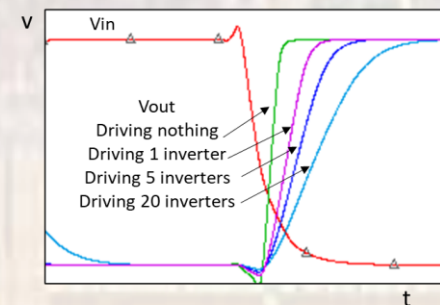
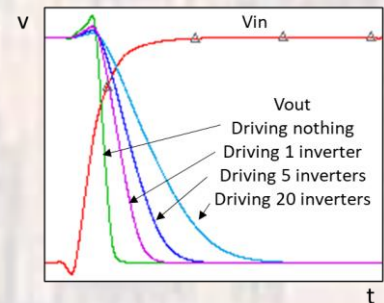
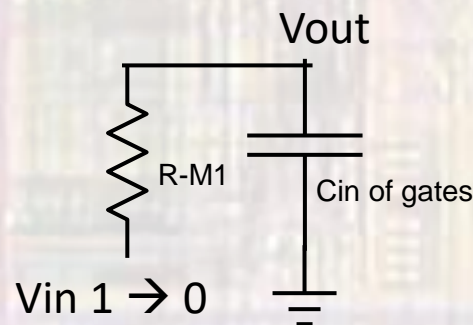
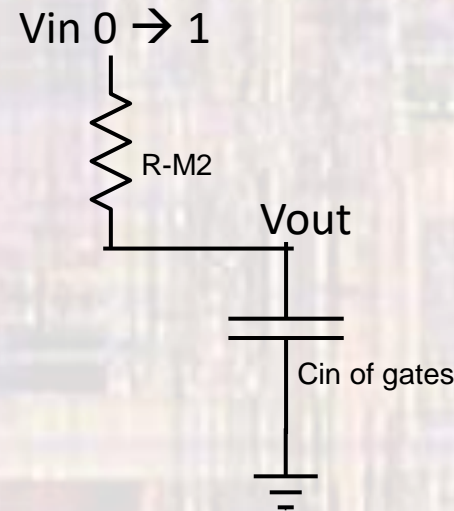
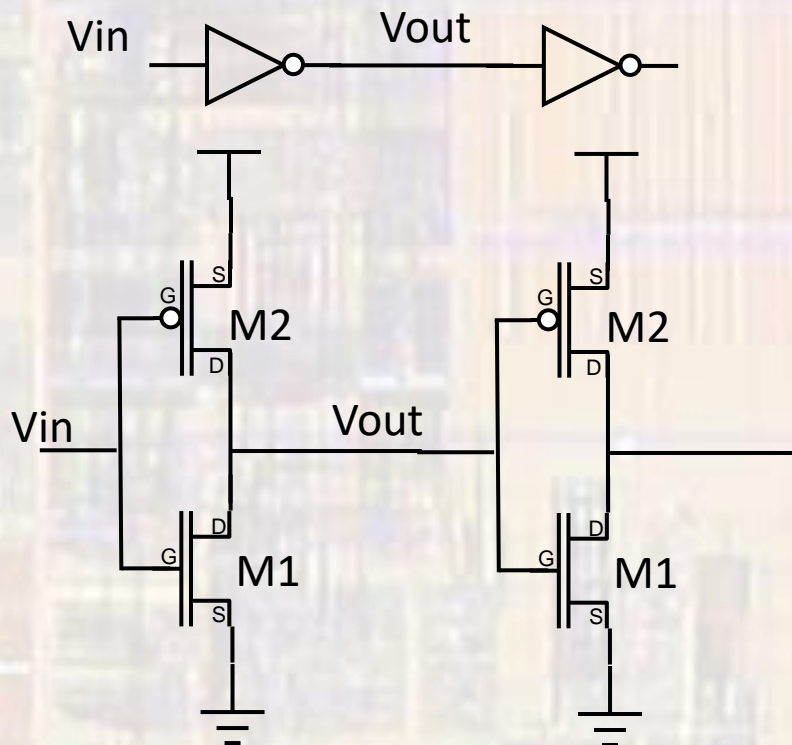
CMOS Timing Characteristics

- CMOS **Transistor Model**
 - Our simplified model of CMOS devices:
 - Transistor D-S path looks like a resistor
 - High valued when off
 - Low valued when on
 - Transistor G looks like a capacitor tied to gnd
 - The D-S resistance can be reduced (increased) by making larger (smaller) devices
 - The G capacitance increases (decreases) for larger(smaller) devices

CMOS Timing Characteristics

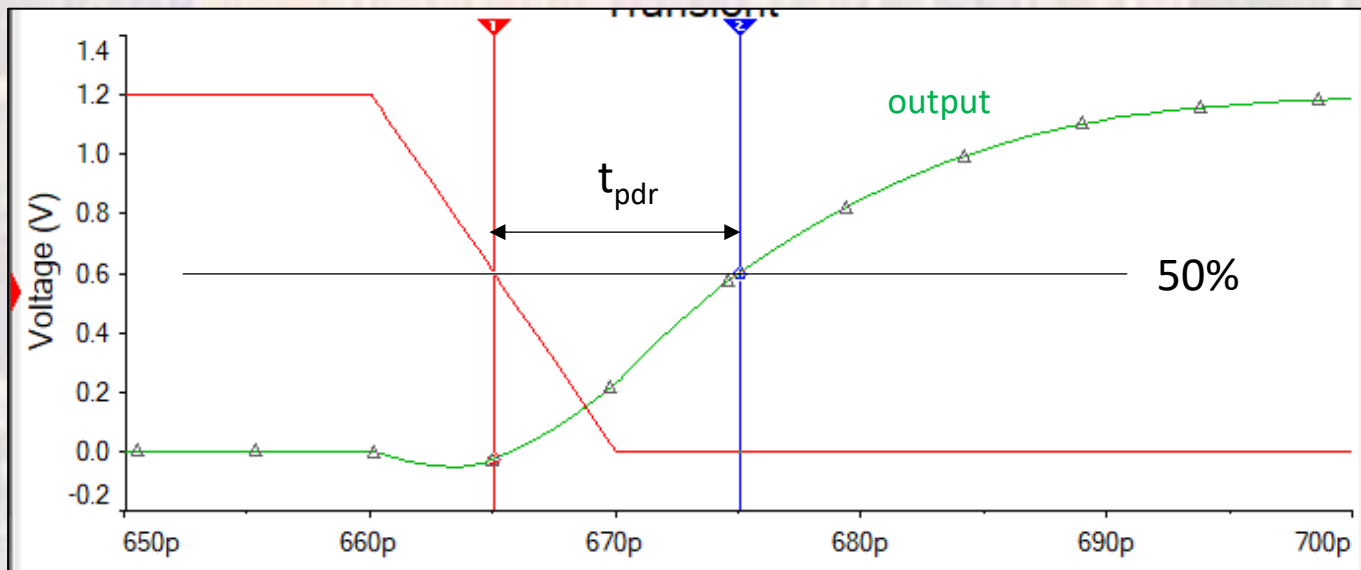
- CMOS **Circuit** Model

- The output of one gate is connected to (drives) one or more gate inputs (Gs)
- This forms an RC circuit



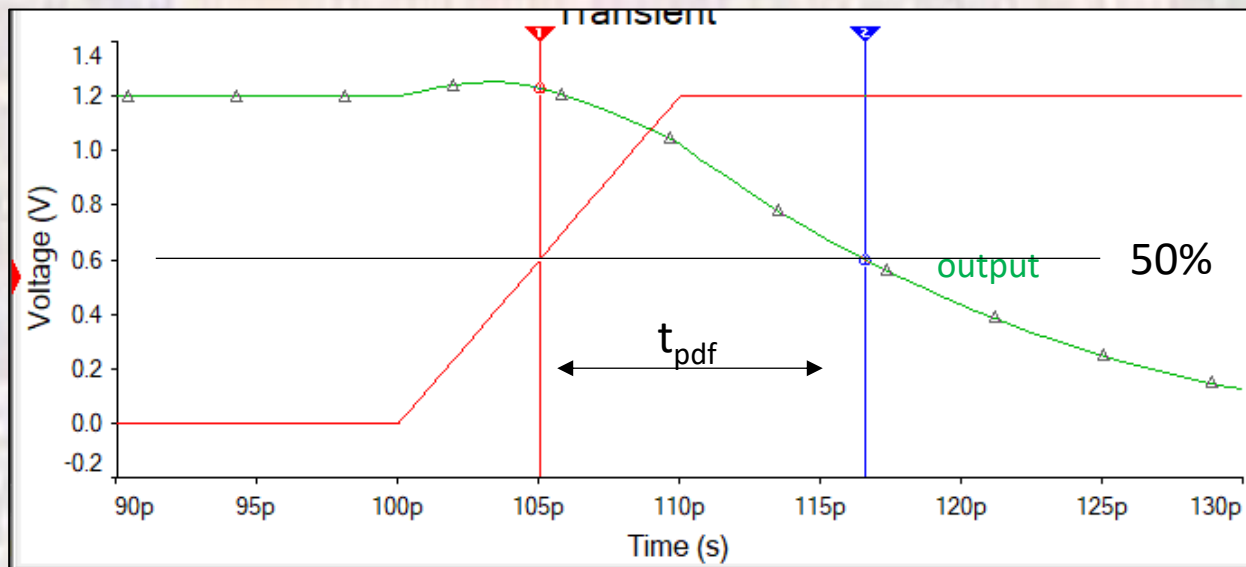
CMOS Timing Characteristics

- Propagation Delay - Rising t_{pdr} t_{pdh}
 - t_{pdr} - Time for Propagation Delay with the output Rising
 - Measured from 50% of **input** “high” value to 50% of **output** “high” value on an output rising edge



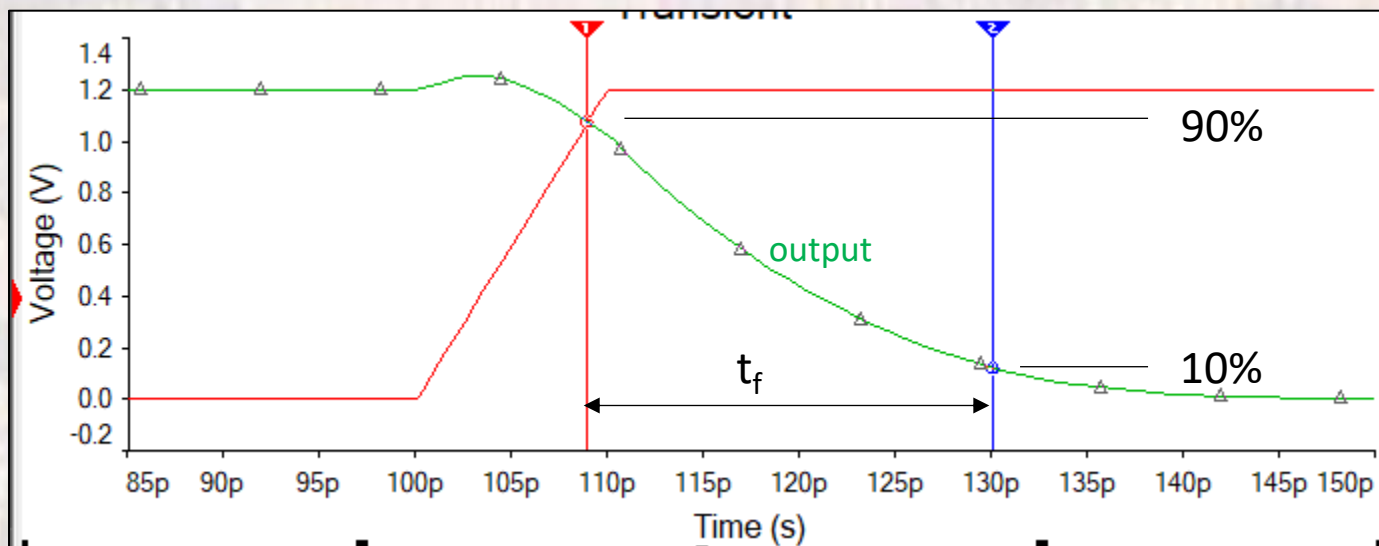
CMOS Timing Characteristics

- Propagation Delay - Falling t_{pdf} t_{pdl}
 - t_{pdf} - Time for Propagation Delay with the output Falling
 - Measured from 50% of **input** “high” value to 50% of **output** “high” value on an output falling edge



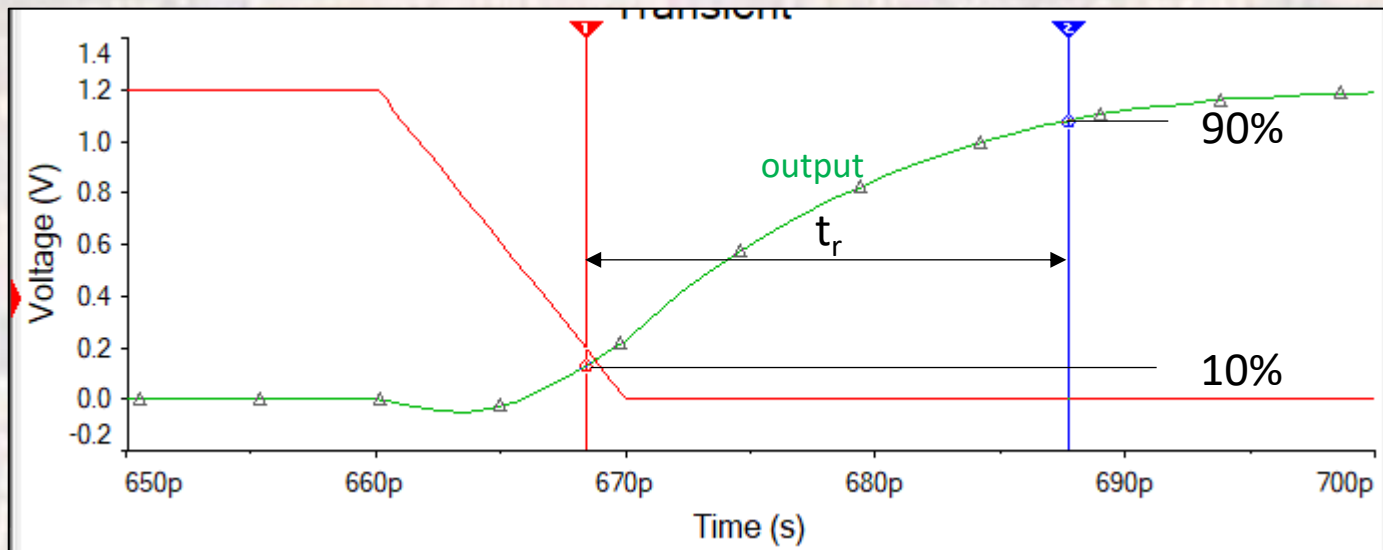
CMOS Timing Characteristics

- Fall Time $t_{\text{fall}} (t_f)$
 - t_f
 - Measured from 90% of “high” value to 10% of “high” value on the **output**



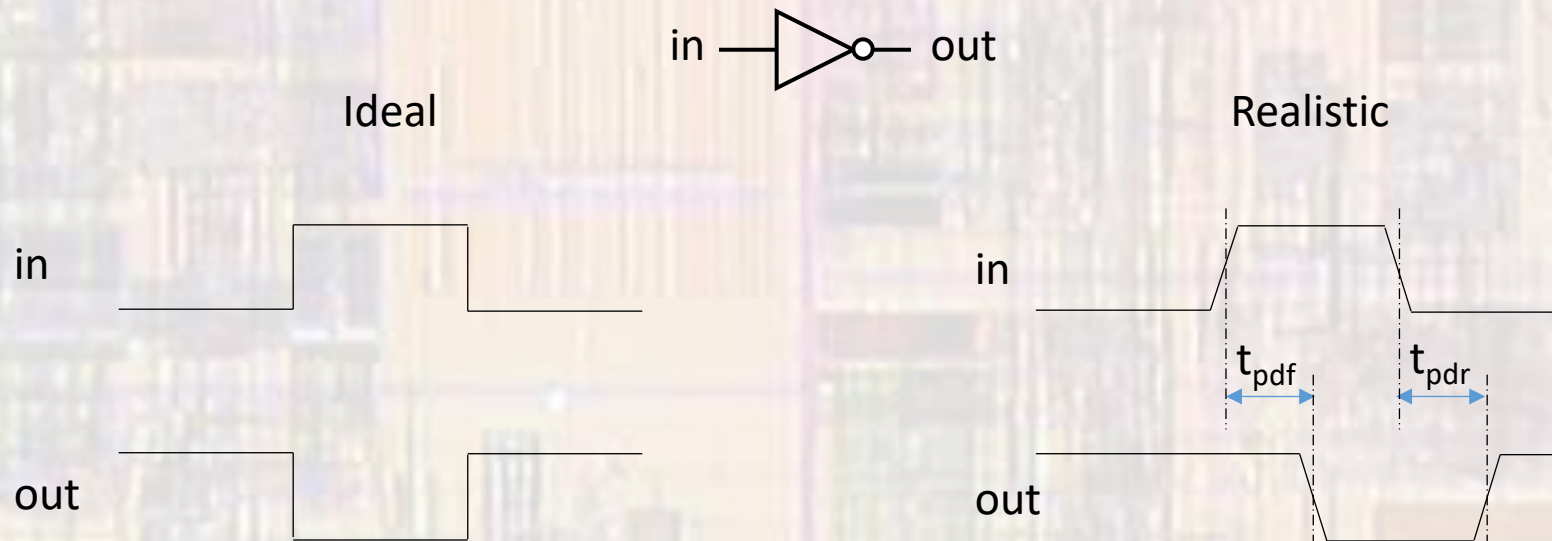
CMOS Timing Characteristics

- Rise Time $t_{\text{rise}} (t_r)$
 - t_r is measured on the output
 - Measured from 10% of “high” value to 90% of “high” value on the **output**



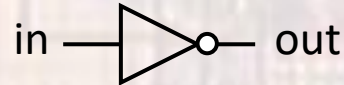
CMOS Timing Characteristics

- Timing Diagrams
 - Propagation Delay
 - **Maximum** time from when the input changes (50%) to the time when the output reaches its **final** value (50%)



CMOS Timing Characteristics

- Timing Diagrams



- Contamination Delay t_{cd}

- **Minimum** time from when the input changes (50%) to the time when the output reaches its **final** value (50%)

- Delay times change due to:

- Circuit parameters
 - Temperature
 - Part to part variations

