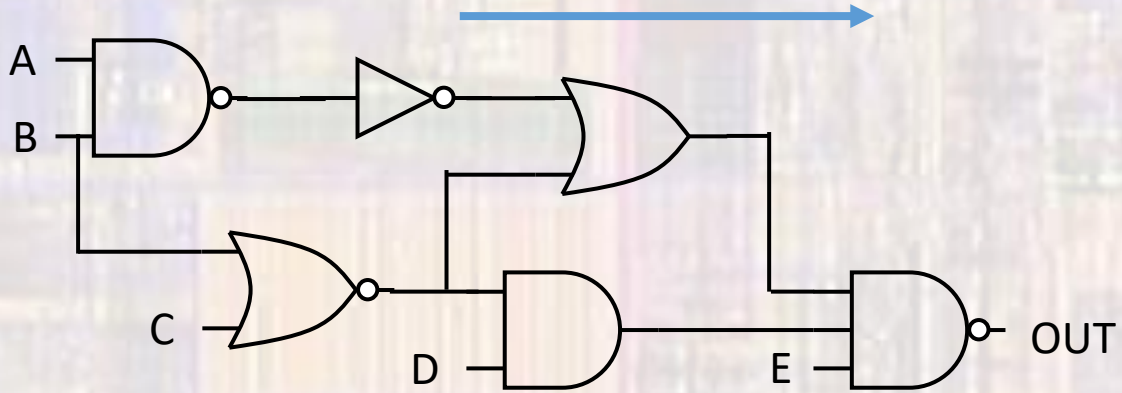
Digital Logic Evaluation Gates

Last updated 10/10/24

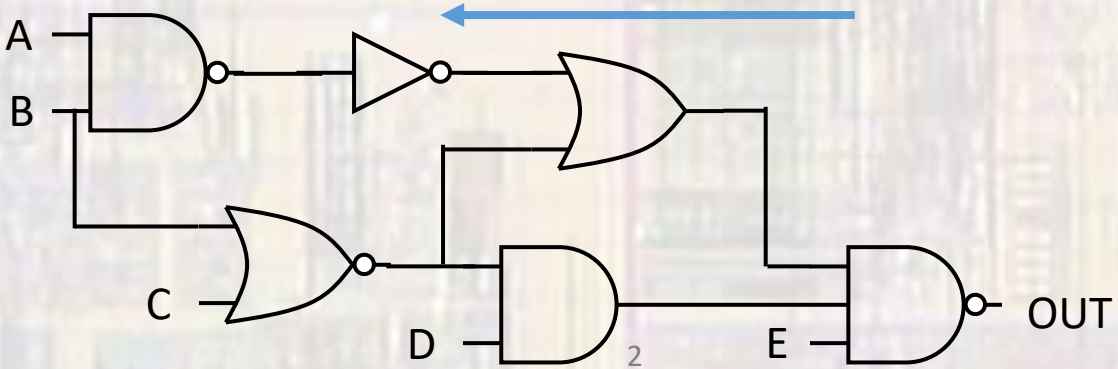
These slides show how to evaluate digital logic circuits via truth tables

Digital Logic Evaluation – Gates

- Circuits are evaluated from input to output when creating truth tables

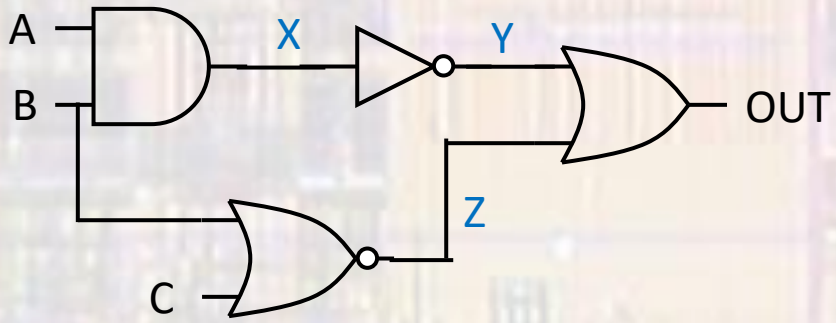


- Circuits are evaluated from output to input when creating logic expressions



Digital Logic Evaluation – Gates

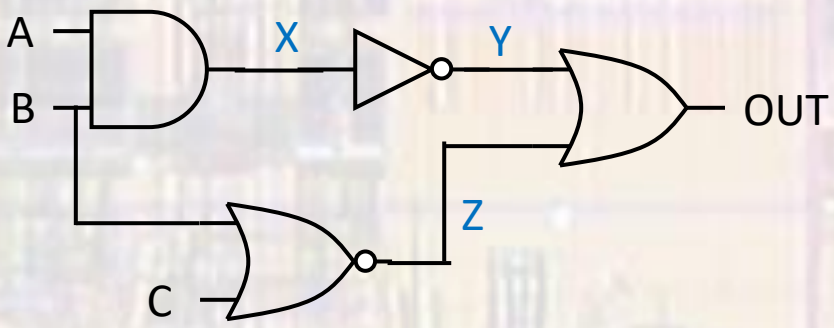
- Logic Evaluation – Gates
  - Truth Table Process
    1. Label all intermediate nodes
    2. Create a truth table that includes all inputs, intermediate nodes and the output – working from input to output
    3. Fill in the table 1 step at a time – working from inputs to output



C	B	A	X (AB)	$\overline{Y}$ ($\overline{X}$)	$\overline{Z}$ ($\overline{B + C}$)	OUT (Y+Z)
0	0	0	0	1	1	1
0	0	1	0	1	1	1
0	1	0	0	1	0	1
0	1	1	1	0	0	0
1	0	0	0	1	0	1
1	0	1	0	1	0	1
1	1	0	0	1	0	1
1	1	1	1	0	0	0

Digital Logic Evaluation – Gates

- Logic Evaluation – Gates
  - Logic Expression Process
    1. Label all intermediate nodes
    2. Starting at the output – write the single gate logic expression
    3. Working from output toward input – substitute each new level's logic gate expression
    4. Reduce as desired



Out = Y + Z
Out = $(\overline{X})$ + (C + B)
Out = $(\overline{AB})$ + $(\overline{C + B})$

Reduction (covered elsewhere)
Out = $\overline{A} + \overline{B} + \overline{B}\,\overline{C}$
OUT = $\overline{A} + \overline{B}$