Digital Logic Reduction Bubble Pushing

Last updated 1/7/25

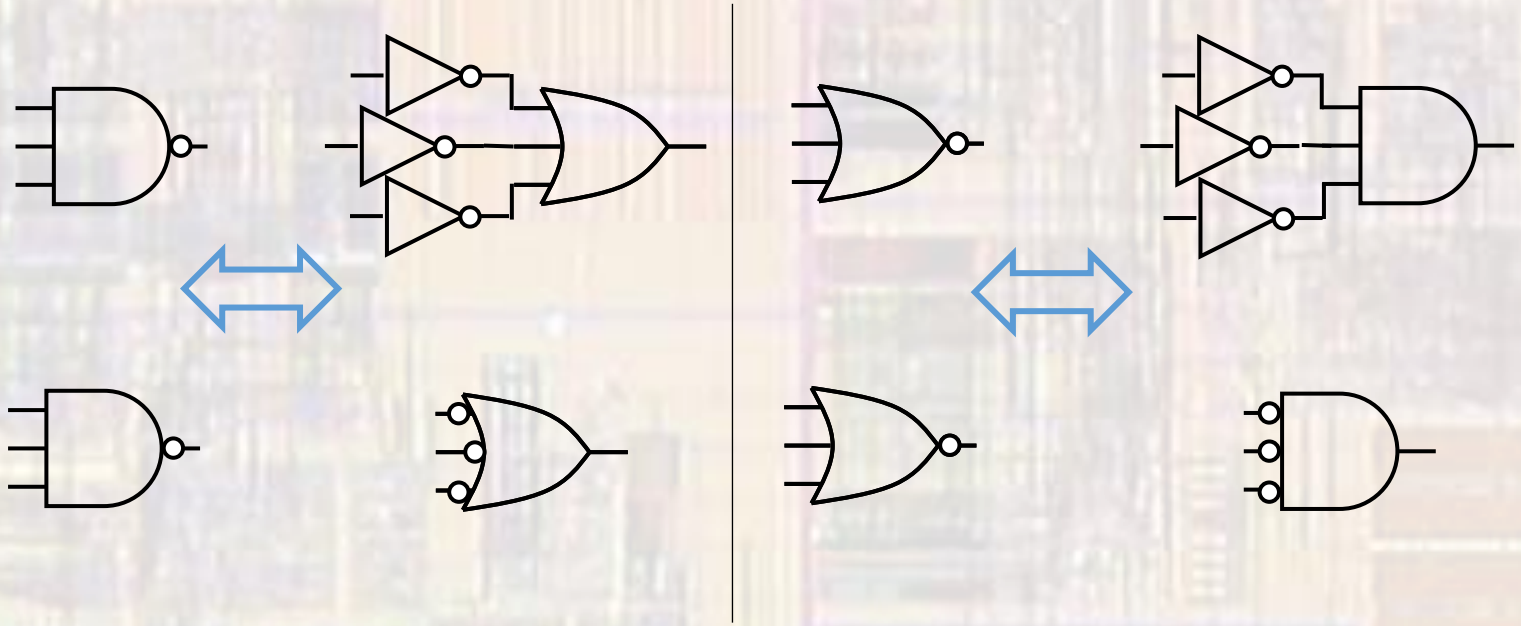
Digital Logic Reduction – bubble pushing

- CMOS NAND and NOR gates are preferred over AND and OR gates
  - Faster
  - Smaller
  - Less Power

Digital Logic Reduction – bubble pushing

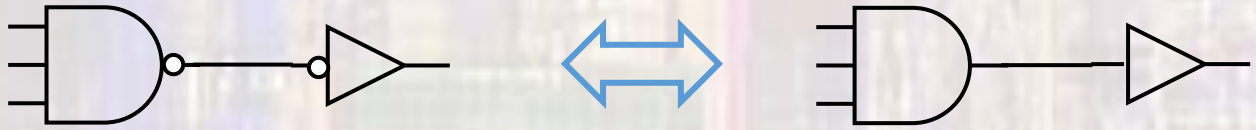
- Use De Morgan's theorem to switch between AND/OR/NAND/NOR
  - Flip the inputs and outputs and swap the gate

T12	$\overline{B_0 \bullet B_1 \bullet B_2 \ldots} = \overline{B}_0 + \overline{B}_1 + \overline{B}_2 \ldots$	$\overline{B_0 + B_1 + B_2 \ldots} = \overline{B}_0 \bullet \overline{B}_1 \bullet \overline{B}_2 \ldots$	DeMorgan's

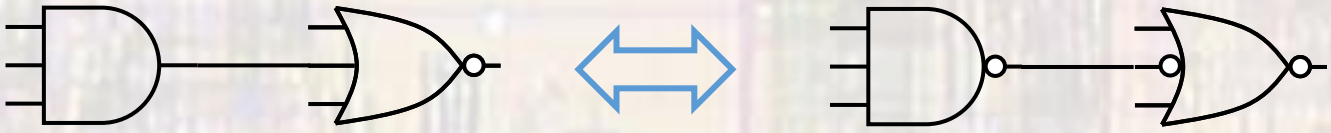


Digital Logic Reduction – bubble pushing

- Bubble Destruction

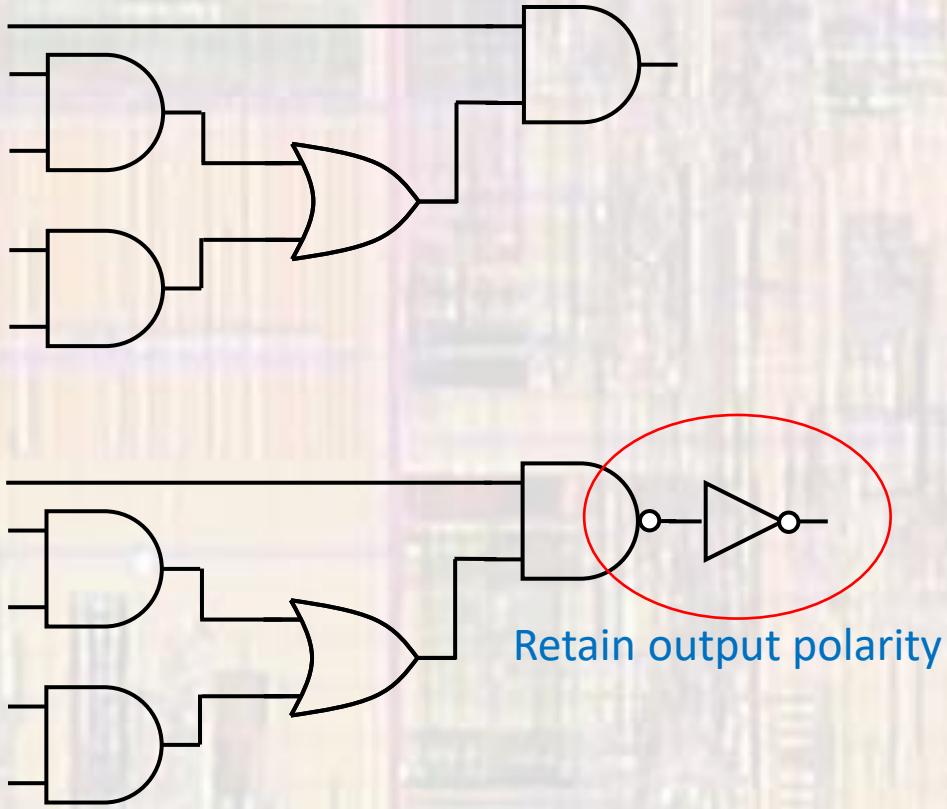


- Bubble Creation



Digital Logic Reduction – bubble pushing

- Example – step 1
  - Convert to NANDs and NORs where possible



Digital Logic Reduction – bubble pushing

- Example – step 2/3