Digital Logic Timing Analysis

Last updated 10/24/24

These slides introduce the basics of a digital logic timing analysis

Digital Logic Timing Analysis

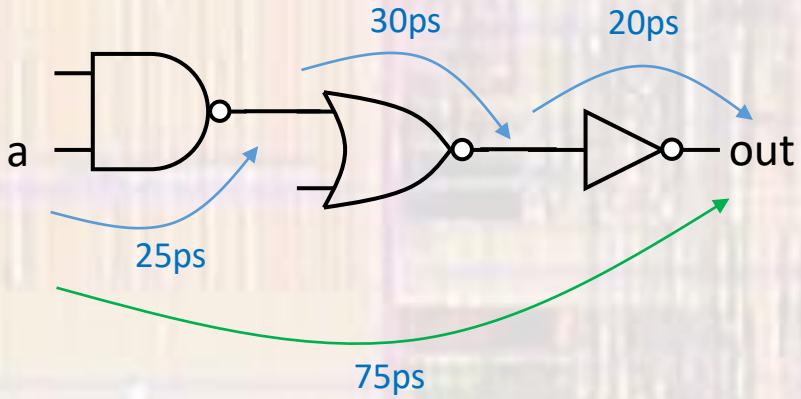
- Digital Logic Gate Library

Gate	Tpd (ps)	Tcd (ps)
INV	20	18
NOR2	30	27
NOR3	40	36
NAND2	25	23
NAND3	35	32

- AND and OR are built from NAND + INV and NOR + INV

Digital Logic Timing Analysis

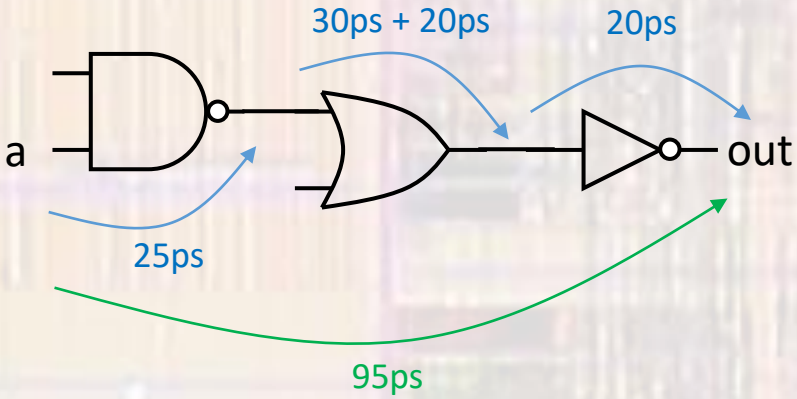
- Example 1 – simple delay calculation
  - Calculate the delay for changes in the a signal to the out signal



t_{pd} = 75ps

Digital Logic Timing Analysis

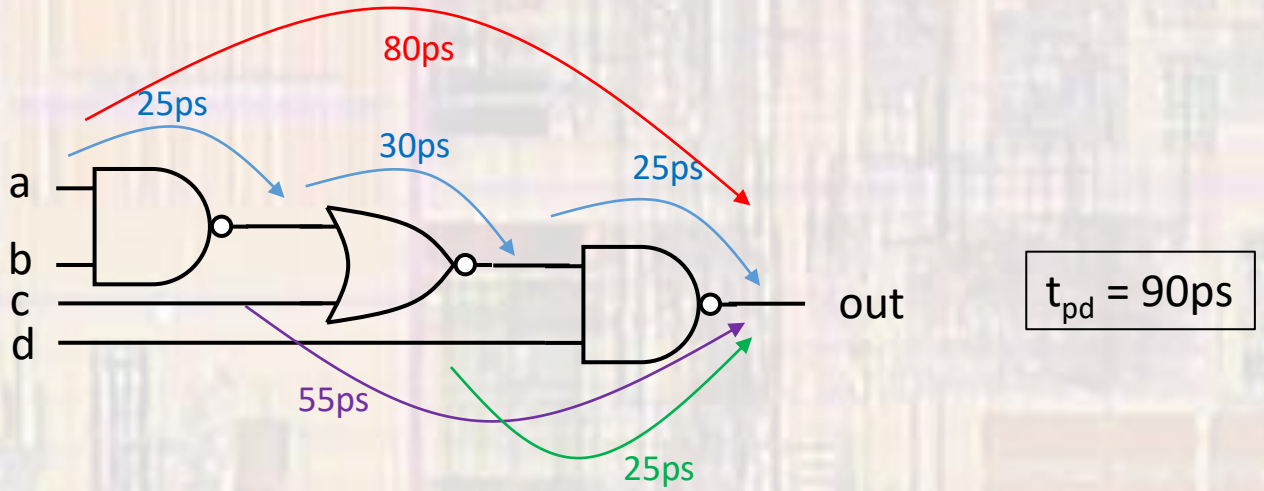
- Example 2 – simple delay calculation
  - Calculate the delay for changes in the a signal to the out signal



t_{pd} = 95ps

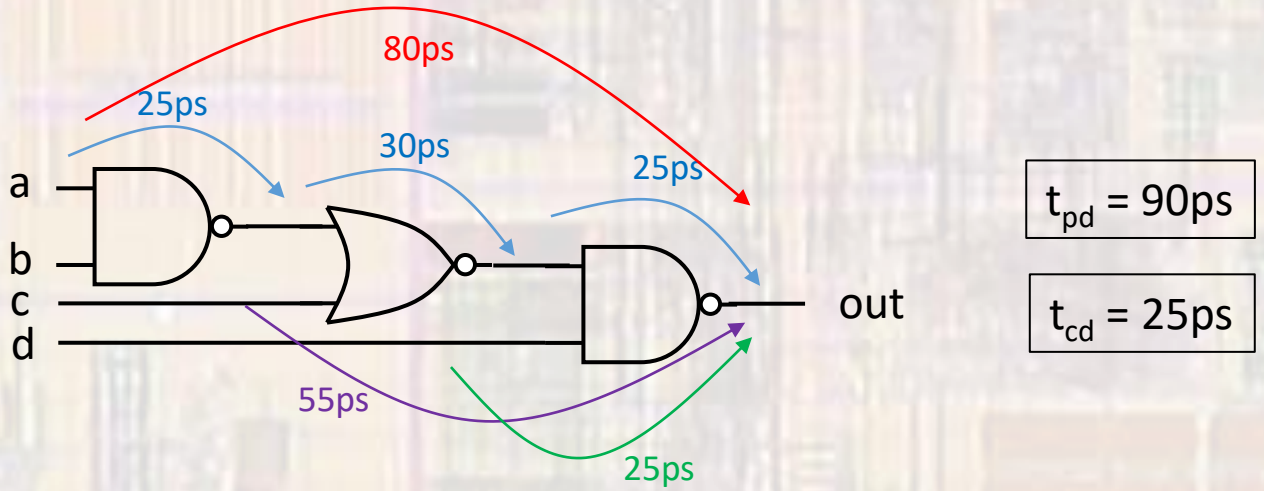
Digital Logic Timing Analysis

- Critical Path
  - The path through a logic circuit that limits the speed at which the circuit operates
    - Always the slowest path
    - Usually (but not always) the longest path



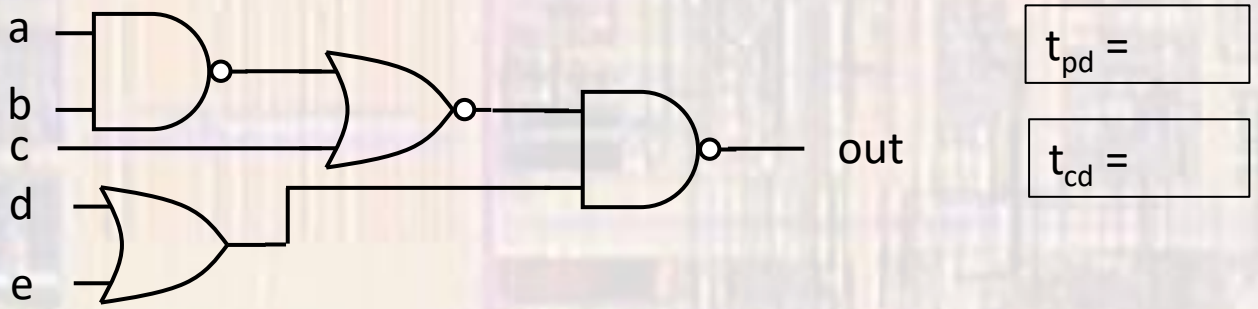
Digital Logic Timing Analysis

- Contamination Path
  - The fastest path through the circuit
    - Always the fastest path
    - Usually (but not always) the shortest path



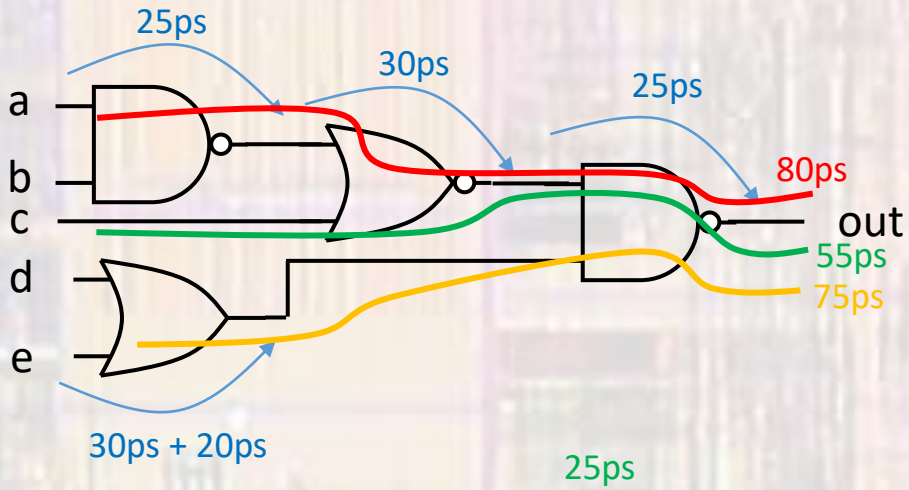
Digital Logic Timing Analysis

- Example 3
  - Find the propagation and contamination delays



Digital Logic Timing Analysis

- Example 3
  - Find the propagation and contamination delays



t_{pd} = 90ps

t_{cd} = 55ps