Digital Logic Timing Glitches

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These slides introduce the basics of a digital logic timing glitches

Digital Logic Timing Glitches

- Digital Logic Timing Glitch
  - A temporary output transition that occurs before the final output value is reached
  - Created when multiple paths lead from 1 input to the output and
    - One implicant in the truth table turns off before another turns on
  - A problem when:
    - We are using the output signal as an edge triggered input
      - More on this later in the class
    - When we look at the result prior to its final value

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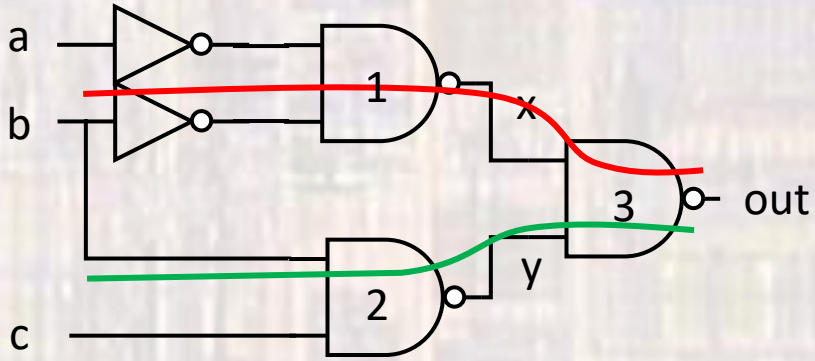
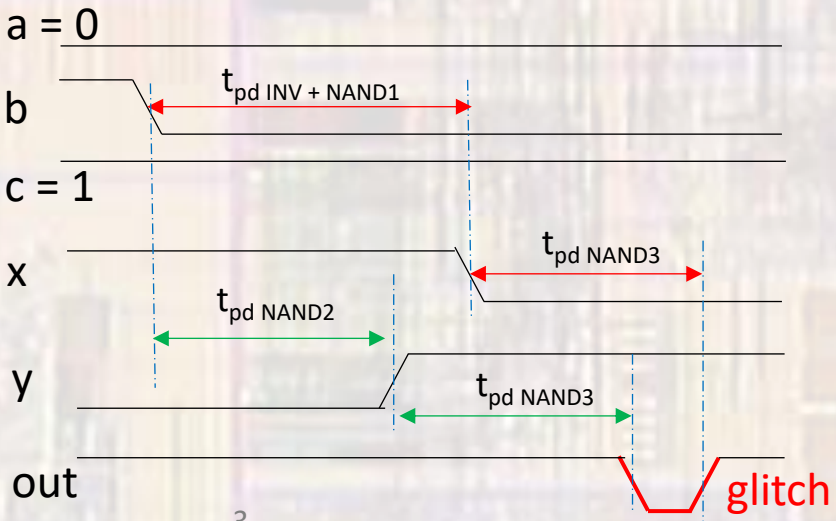
- Example 1 – input transition that should not cause an output change

a	b	c	OUT
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1



a = 0
c = 1
b: 1 or 0
out = 1



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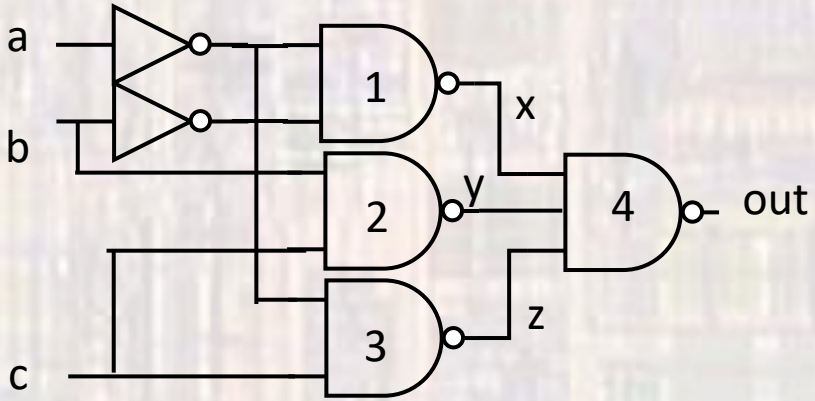
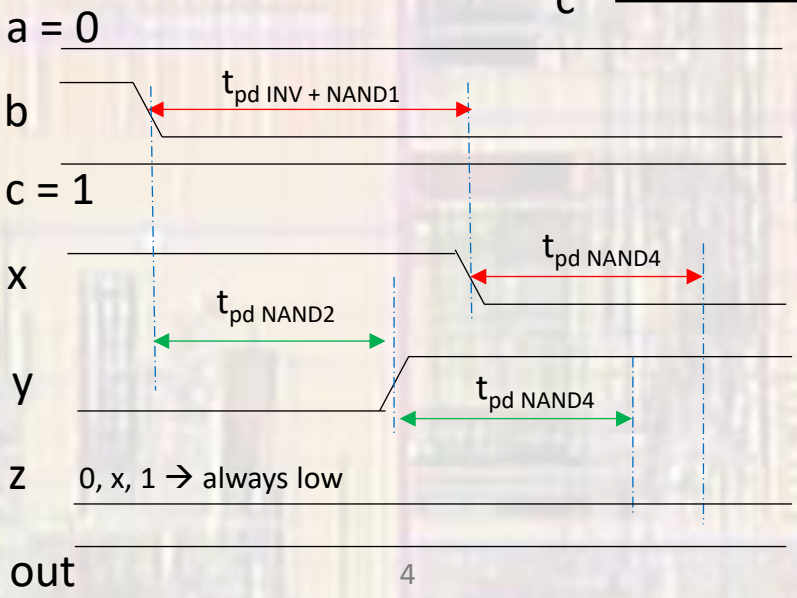
- Example 2 – glitch free solution
  - Use the consensus theorem to ensure no glitches (more later)
  - Bigger solution – no glitches





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