Flip-Flop Basics

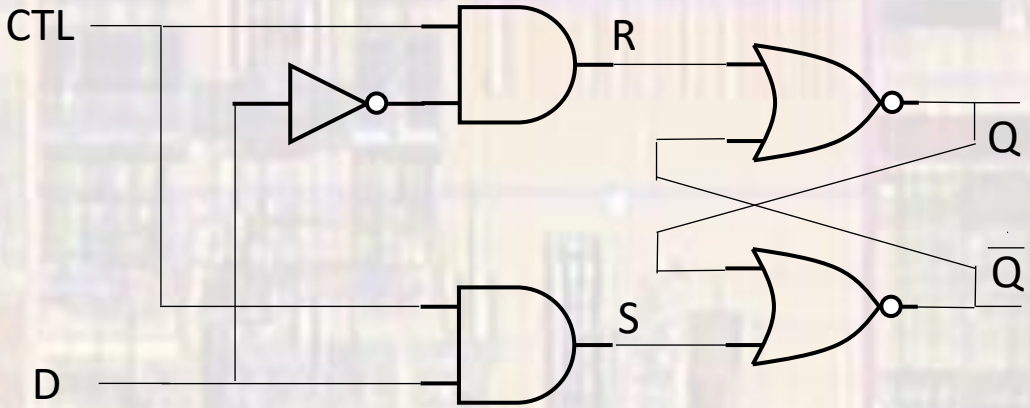
Last updated 10/24/24

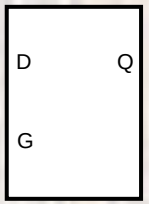
Flip-Flop Basics

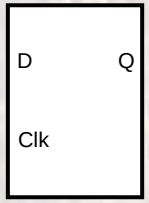
- D Latch (data)

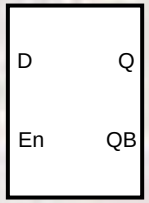
Level Sensitive Latch

CTL = low → latched
CTL = high → Transfer





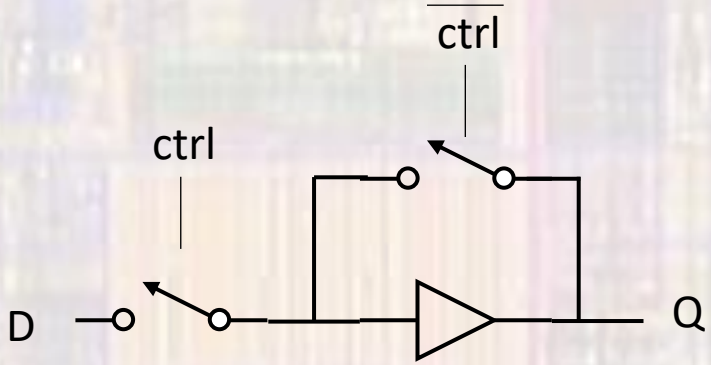




CTL	D	Q
0	x	Q_{old}
1	D	D

Flip-Flop Basics

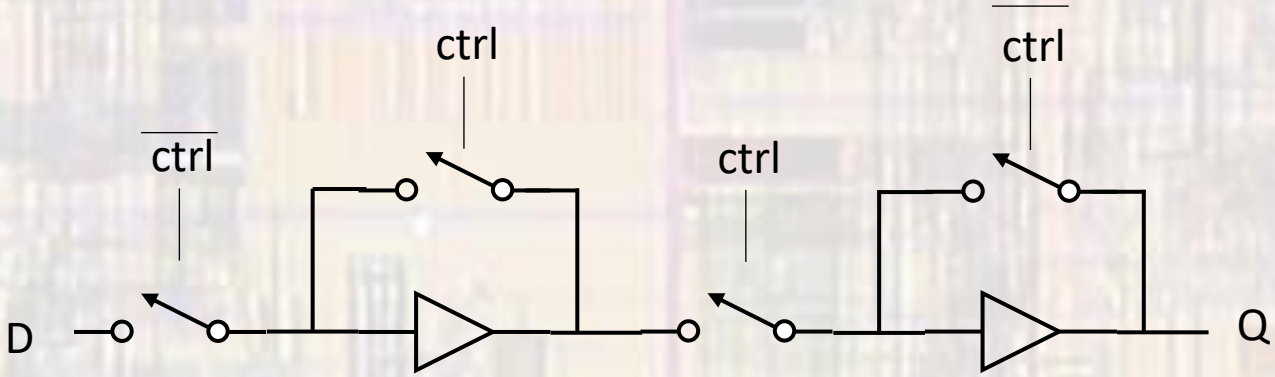
- D Latch - Abstraction



CTRL	D	Q
0	x	Q_{old}
1	D	D

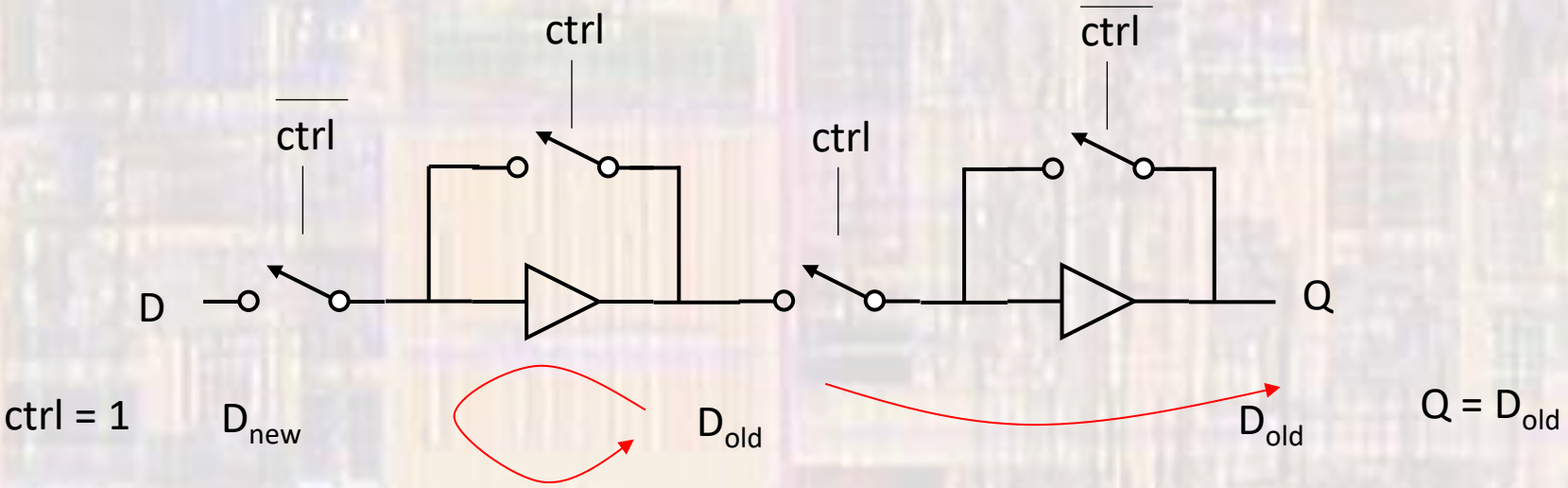
Flip-Flop Basics

- D Flip-Flop – Abstraction
  - 2 series D-Latches with opposite control polarity
  - Synchronous Sequential Circuit
    - Sequential - Output depends on inputs and 1 state variable Q (Q_{old})
    - Synchronous – output changes limited to specific input conditions
      - Typically, on a (rising) clk edge
    - Memory is in the bi-stable latch



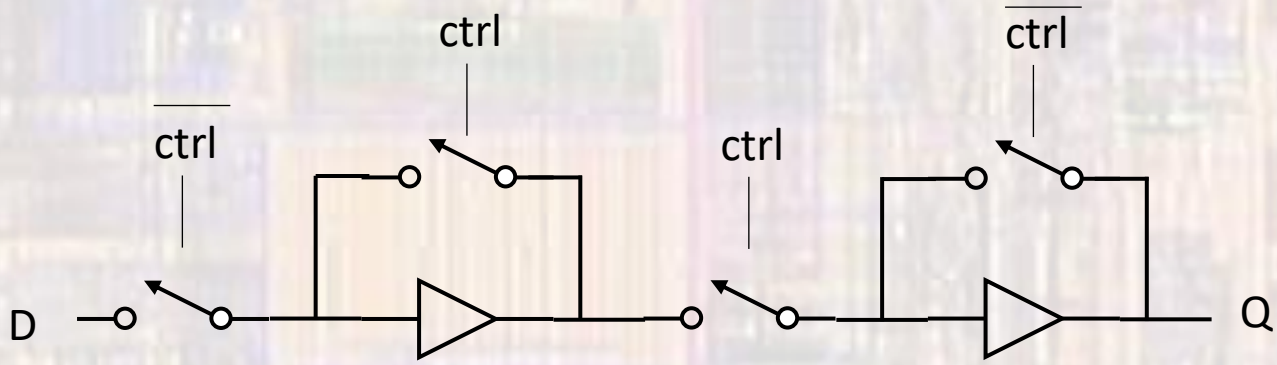
Flip-Flop Basics

- D Flip-Flop – Abstraction
  - 2 series D-Latches with opposite control polarity



Flip-Flop Basics

- D Flip-Flop – Abstraction
  - 2 series D-Latches with opposite control polarity



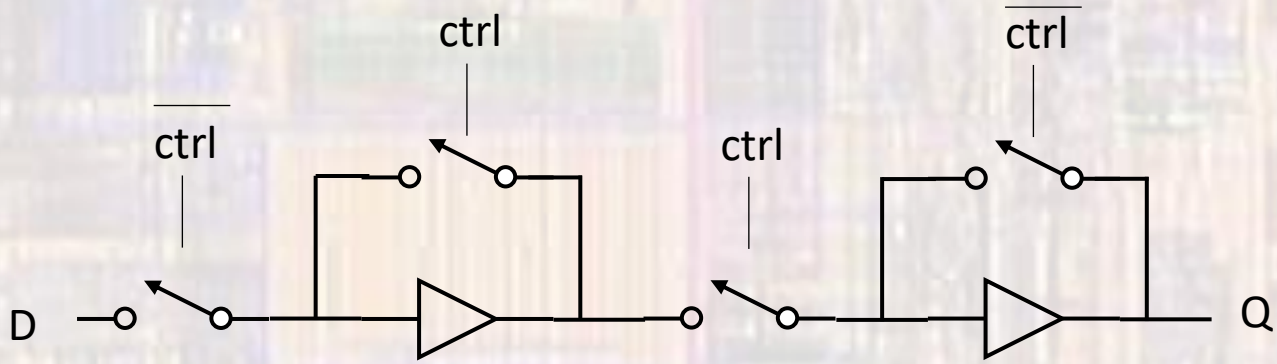
ctrl = 1 D_{new} D_{old} D_{old} $Q = D_{old}$

fast

ctrl = ↓ D_{new} slow D_{new} D_{old} D_{old} $Q = D_{old}$

Flip-Flop Basics

- D Flip-Flop – Abstraction
  - 2 series D-Latches with opposite control polarity



ctrl = 1 D_{new} D_{old} D_{old} $Q = D_{old}$

fast

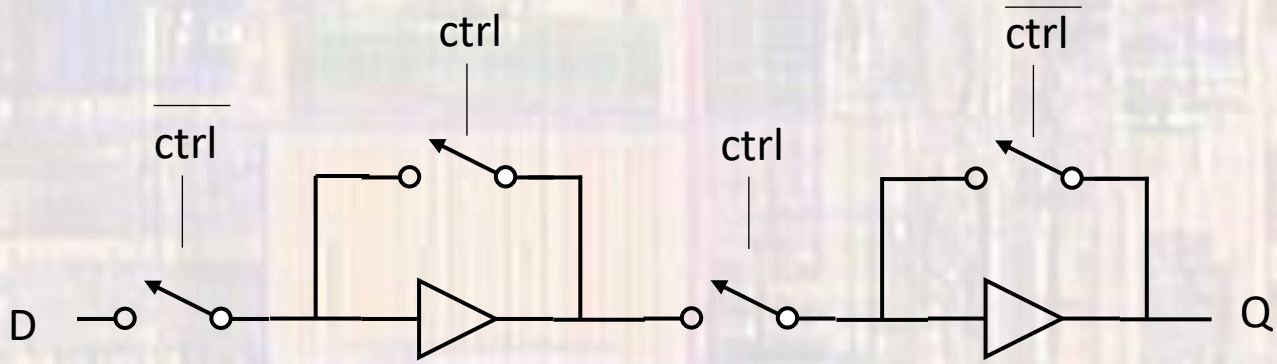
slow

ctrl = ↓ D_{new} D_{new} D_{old} D_{old} $Q = D_{old}$

ctrl = 0 D_{new} D_{new} D_{old} D_{old} $Q = D_{old}$

Flip-Flop Basics

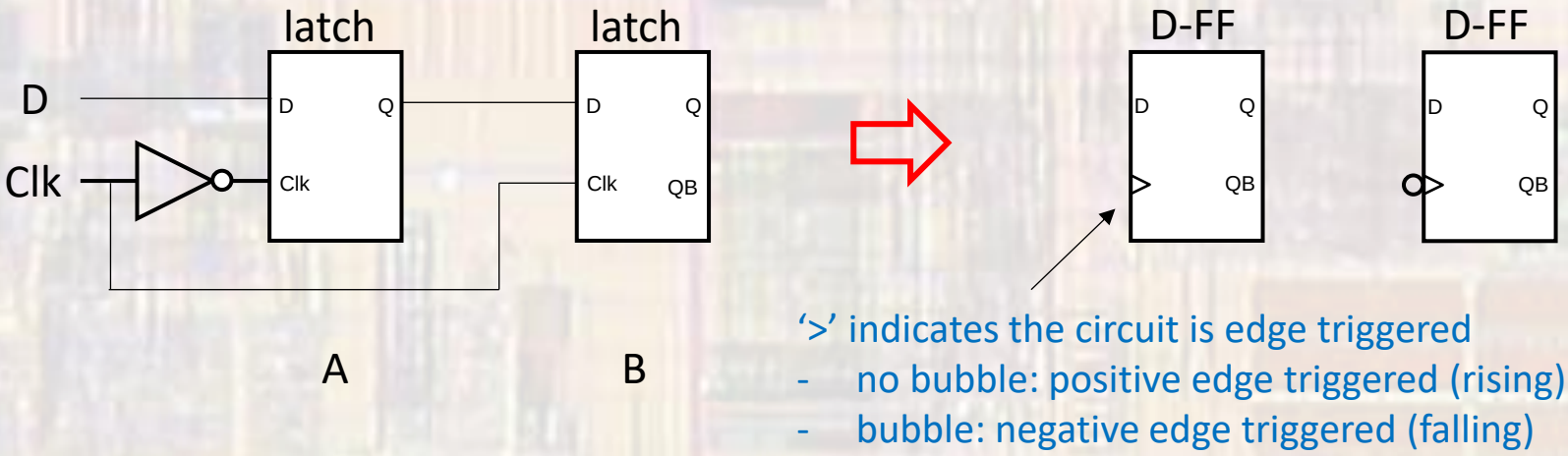
- D Flip-Flop – Abstraction
  - 2 series D-Latches with opposite control polarity



ctrl = 1	D_{new}	D_{old}		D_{old}	$Q = D_{old}$
ctrl = ↓	D_{new}	slow ↓ D_{new}	D_{old}	fast ↓ D_{old}	$Q = D_{old}$
ctrl = 0	D_{new}	D_{new}	D_{old}	D_{old}	$Q = D_{old}$
ctrl = ↑	D_{new}	fast ↓ D_{new}		slow ↓ D_{new}	$Q = D_{new}$

Flip-Flop Basics

- D Flip-Flop (data)
  - Synchronous Sequential Circuit
    - Sequential - Output depends on inputs and 1 state variable Q (Q_{old})
    - Synchronous – output changes limited to specific input conditions
      - Typically, on a (rising) clk edge
    - Memory is in the bi-stable latch

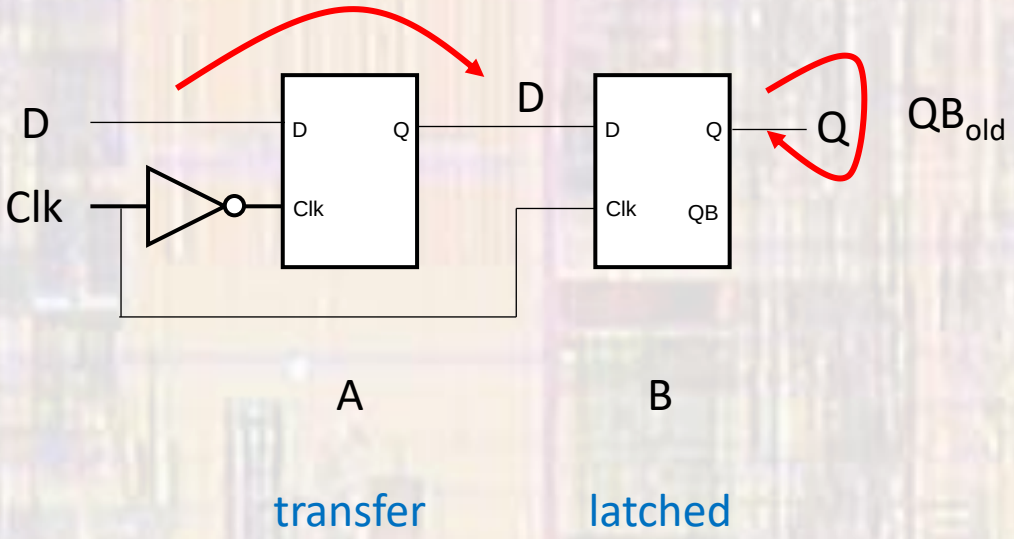


Flip-Flop Basics

D-Latch

CTL CLK	D	Q
0	x	Q_{old}
1	D	D

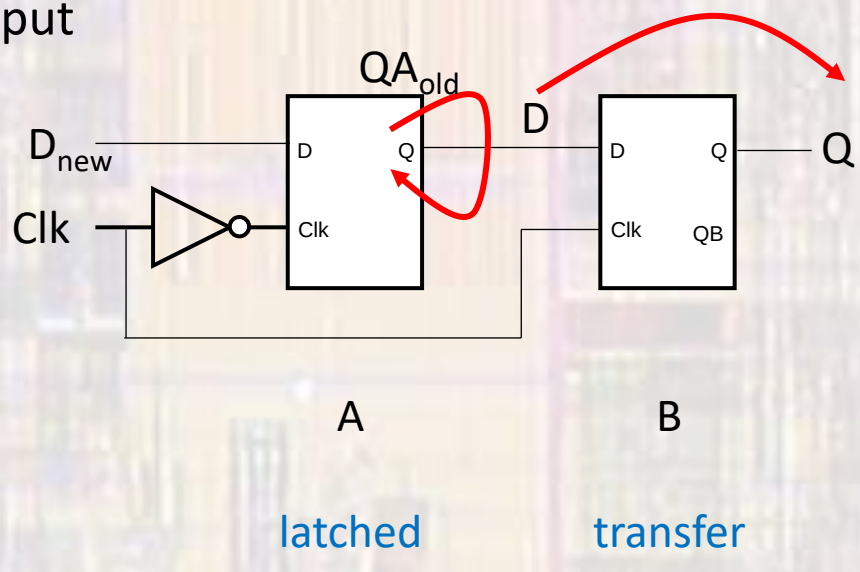
- D Flip-Flop (data)
  - Clock low – after a short time
    - A is enabled and passes D to it's Q output
    - B is in latch mode and retains it's state - QB_{old}



D	Clk	Q
x	0	QB_{old}

Flip-Flop Basics

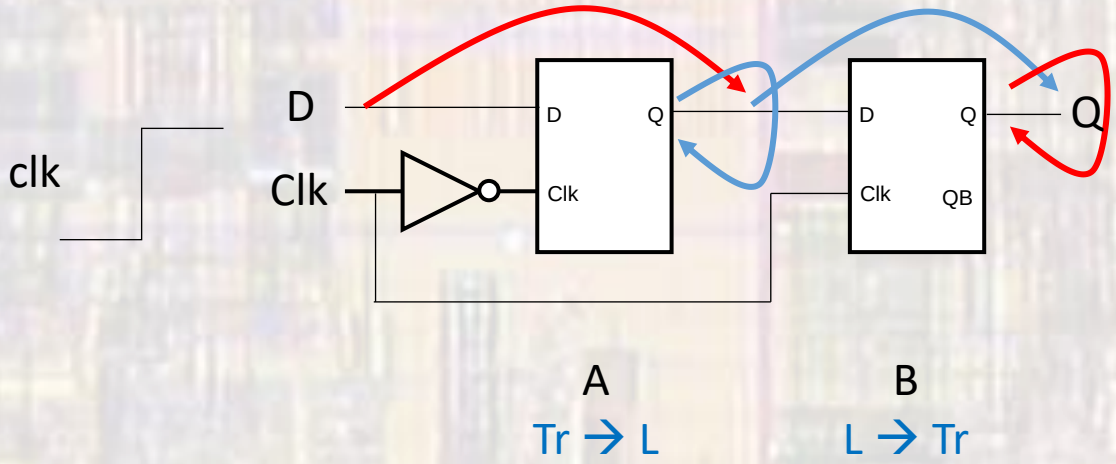
- D Flip-Flop (data)
  - Clock high – after a short time
    - A is latched and retains it's state – QA_{old} (original value of D)
    - B is in transfer mode and would have already passed D to it's Q output



D	Clk	Q
x	0	QB_{old}
x	1	QA_{old} (D_{old})

Flip-Flop Basics

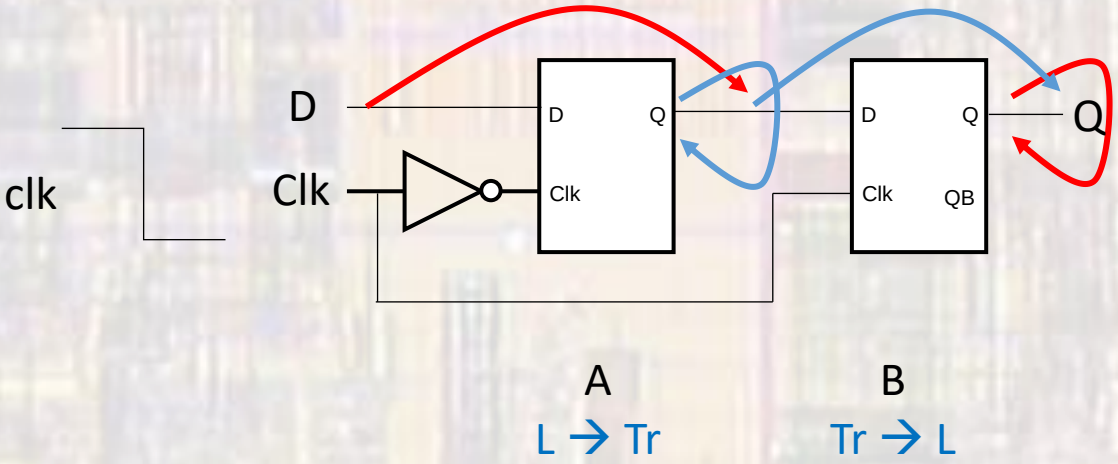
- D Flip-Flop (data)
  - Clock Low → High
    - D has previously been passed to the intermediate node
    - When clk transitions high, the intermediate value (D) is passed to the output while simultaneously the A becomes latched
    - Further changes of the D input are blocked by the latched A



D	Clk	Q
x	0	QB_{old}
x	1	QA_{old}
D	↑	D

Flip-Flop Basics

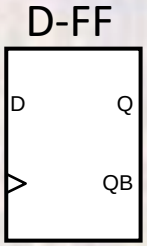
- D Flip-Flop (data)
  - Clock High → Low
    - The output is latched by the B
    - The new D input is allowed to transfer to the intermediate node but no further



D	Clk	Q
x	0	QB_{old}
x	1	QA_{old}
D	↑	D
x	↓	QA_{old}

Flip-Flop Basics

- D Flip-Flop (data)
  - Truth Table
    - Positive Edge Triggered D Flip-Flop
      - (typically, just called a D Flip-flop)



D	Clk	Q
x	0	Q_{old}
x	1	Q_{old}
D	↑	D
x	↓	Q_{old}