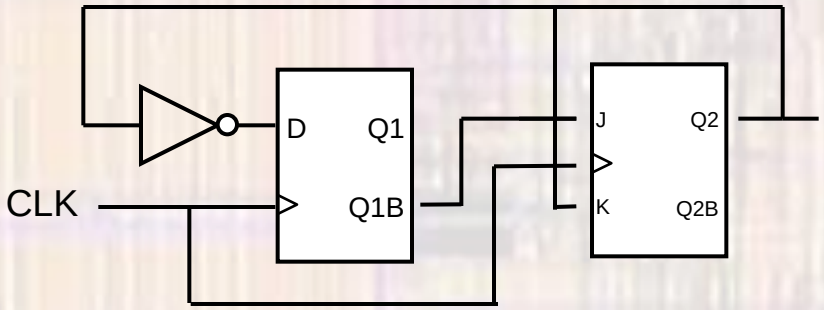
Flip-Flop Circuit Analysis

Last updated 11/12/24

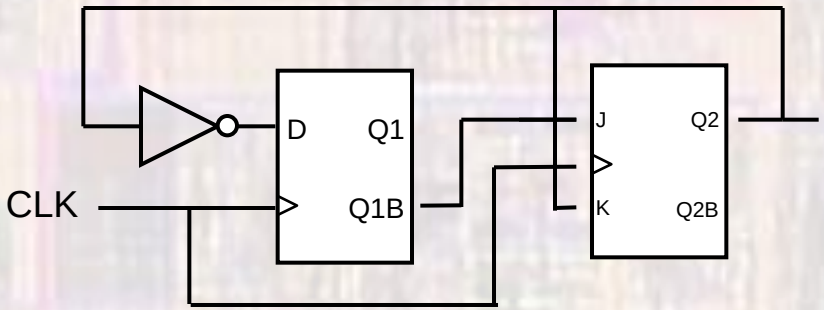
Flip-Flop Circuit Analysis

- Flip-Flops - Example



Flip-Flop Circuit Analysis

- Flip-Flops - Example



Initial State

D	J	K	Q1	Q1B	Q2	Q2B
Initial						
			1			0
After clk1						
After clk2						
After clk3						

You must know these to analyze the circuit

Flip-Flop Circuit Analysis

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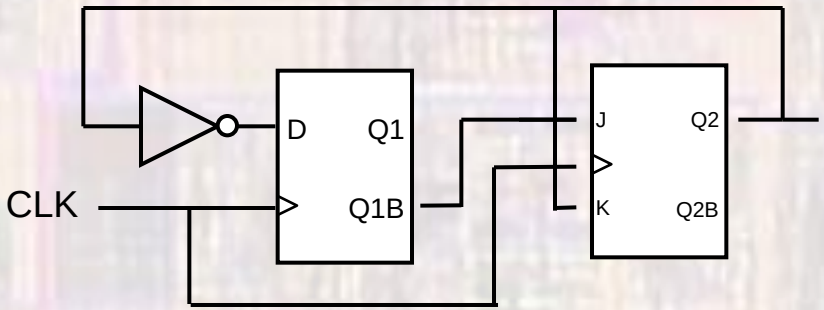


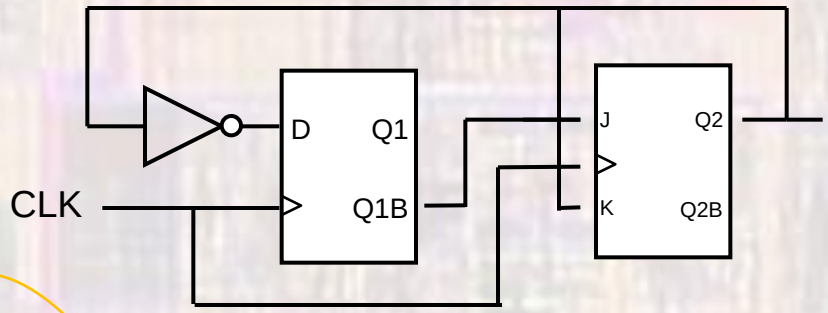
Initial State

D	J	K	Q1	Q1B	Q2	Q2B
Initial						
			1	0	1	0
After clk1						
After clk2						
After clk3						

known

Flip-Flop Circuit Analysis

- Flip-Flops - Example



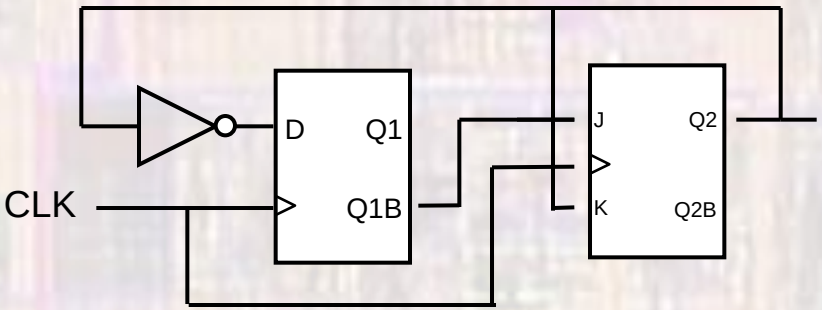
Initial State

D	J	K	Q1	Q1B	Q2	Q2B
Initial						
0	0	1	1	0	1	0
After clk1						
After clk2						
After clk3						

Asynchronous

Flip-Flop Circuit Analysis

- Flip-Flops - Example



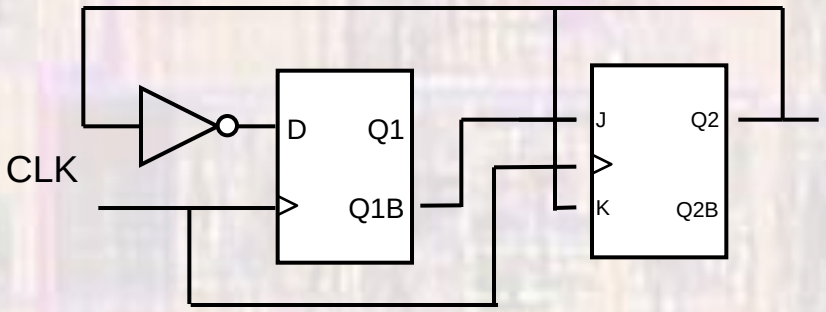
Clk

Synchronous Propagation

D	J	K	Q1	Q1B	Q2	Q2B
Initial						
0	0	1	1	0	1	0
After clk1						
			0	1	0	1
After clk2						
After clk3						

Flip-Flop Circuit Analysis

- Flip-Flops - Example

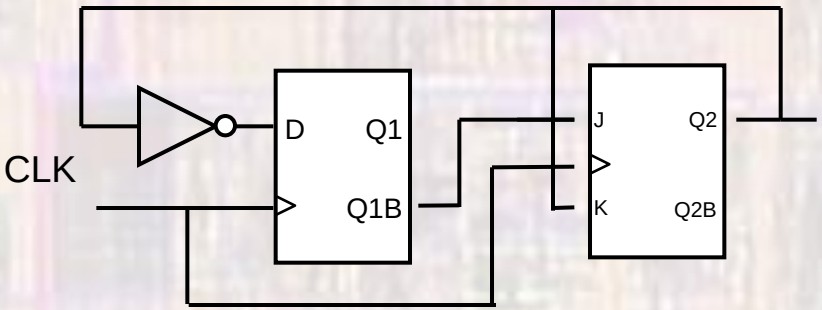


Asynchronous Propagation

D	J	K	Q1	Q1B	Q2	Q2B
Initial						
0	0	1	1	0	1	0
After clk1						
			0	1	0	1
1	1	0				
After clk2						
After clk3						

Flip-Flop Circuit Analysis

- Flip-Flops - Example



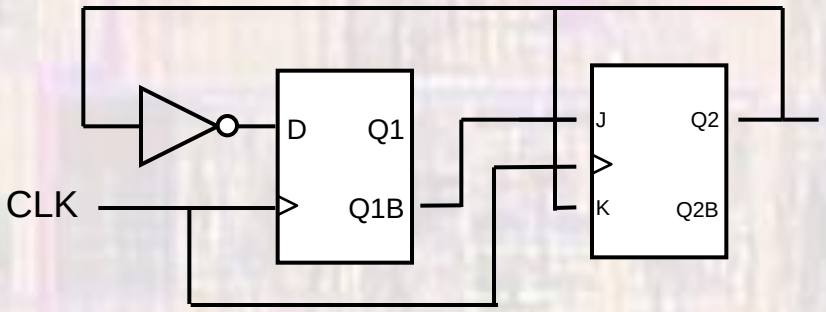
Clk

Synchronous Propagation

D	J	K	Q1	Q1B	Q2	Q2B
Initial						
0	0	1	1	0	1	0
After clk1						
			0	1	0	1
1	1	0				
After clk2						
			1	0	1	0
After clk3						

Flip-Flop Circuit Analysis

- Flip-Flops - Example

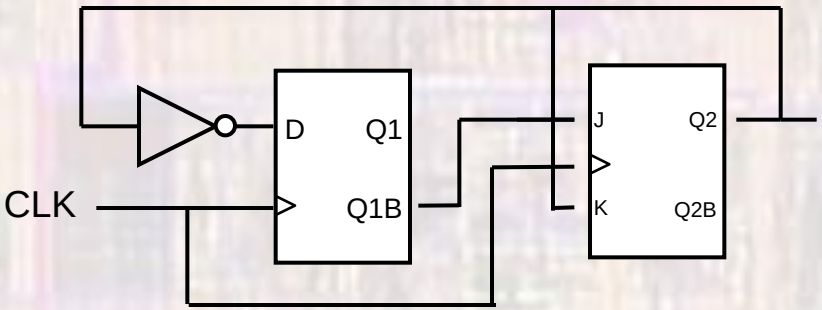


Asynchronous Propagation

D	J	K	Q1	Q1B	Q2	Q2B
Initial						
0	0	1	1	0	1	0
After clk1						
			0	1	0	1
1	1	0				
After clk2						
			1	0	1	0
0	0	1				
After clk3						

Flip-Flop Circuit Analysis

- Flip-Flops - Example



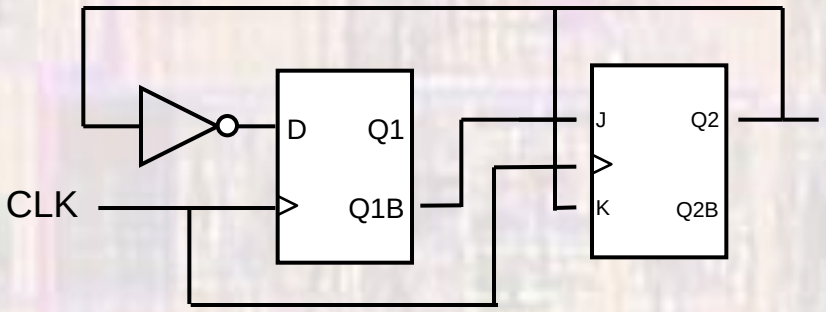
Clk

Synchronous Propagation

D	J	K	Q1	Q1B	Q2	Q2B
Initial						
0	0	1	1	0	1	0
After clk1						
			0	1	0	1
1	1	0				
After clk2						
			1	0	1	0
0	0	1				
After clk3						
			0	1	0	1

Flip-Flop Circuit Analysis

- Flip-Flops - Example

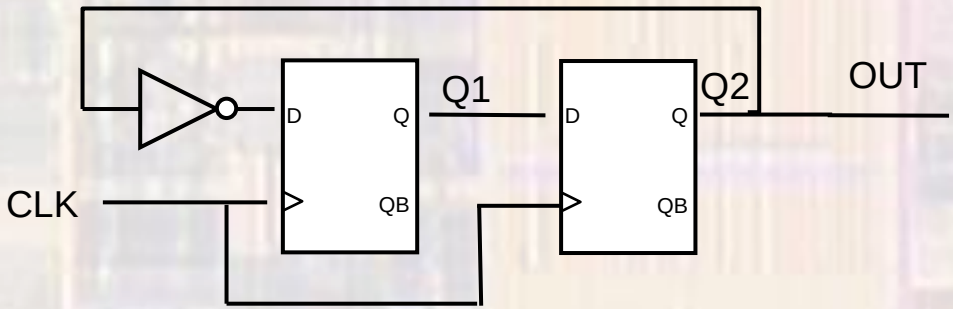


Asynchronous Propagation

D	J	K	Q1	Q1B	Q2	Q2B
Initial						
0	0	1	1	0	1	0
After clk1						
			0	1	0	1
1	1	0				
After clk2						
			1	0	1	0
0	0	1				
After clk3						
			0	1	0	1
1	1	0				

Flip-Flop Circuit Analysis

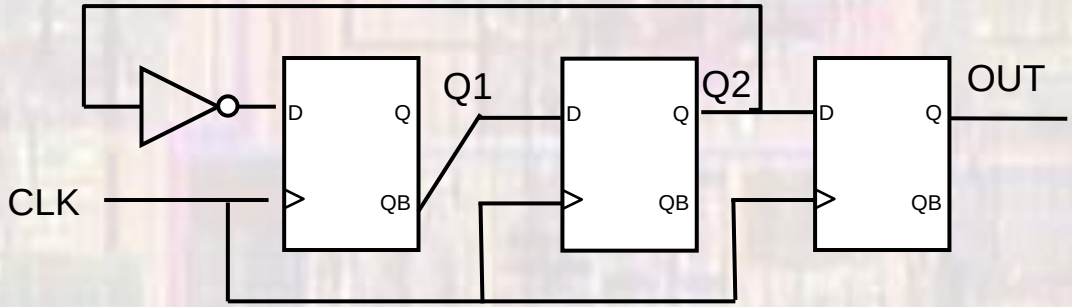
- Example – 2
  - Assume all Flip-Flops have been reset



	D1	D2	Q1	Q2	OUT
Initial			0	0	0
async	1	0			
After Clk 1			1	0	0
async	1	1			
After Clk 2			1	1	1
async	0	1			
After Clk 3			0	1	1
async	0	0			
After Clk 4			0	0	0
async	1	0			
After Clk 5			1	0	0
async	1	1			
After Clk 6			1	1	1
async	0	1			

Flip-Flop Circuit Analysis

- Example – 3
  - Assume all reset



	D1	D2	D3	Q1	Q1B	Q2	OUT
Initial				0	1	0	0
async	1	1	0				
After Clk 1				1	0	1	0
async	0	0	1				
After Clk 2				0	1	0	1
async	1	1	0				
After Clk 3				1	0	1	0
async	0	0	1				
After Clk 4				0	1	0	1
async	1	1	0				
After Clk 5				1	0	1	0
async	0	0	1				
After Clk 6				0	1	0	1
async	1	1	0				