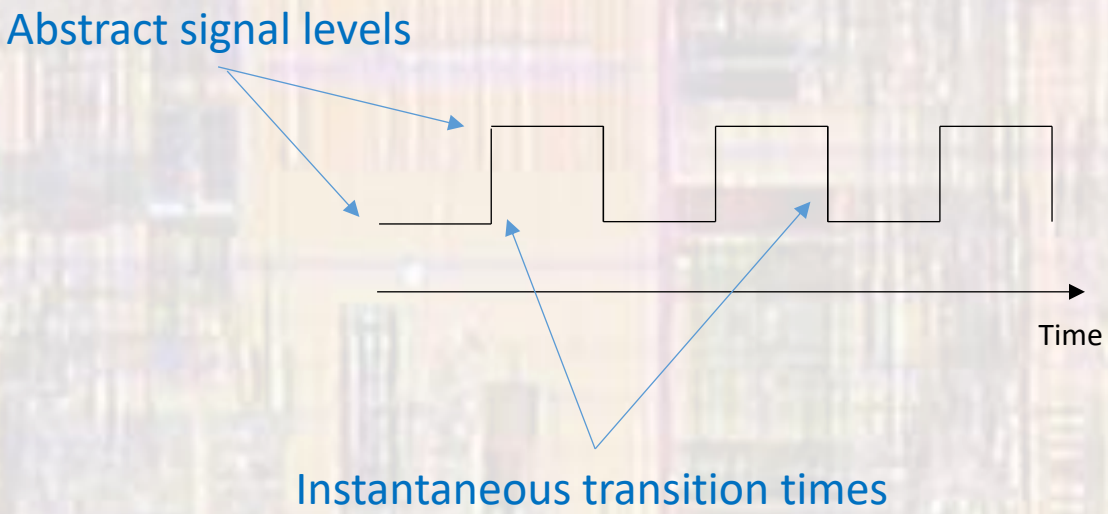
Gate Level Signal Diagrams

Last updated 10/16/24

These slides show how to draw signal diagrams from gate schematics

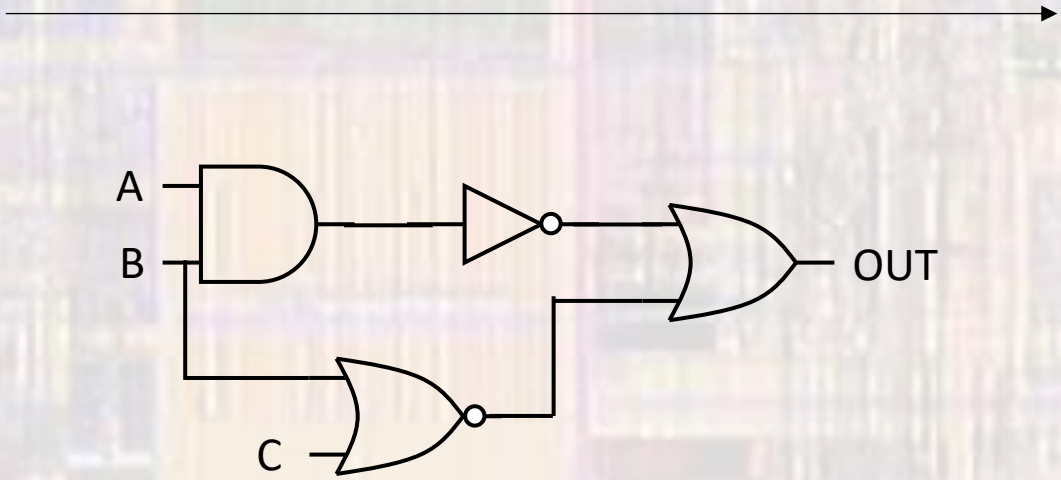
Gate Level Signal Diagrams

- Signal Diagram
  - A simplified drawing of time domain signal changes
    - Abstract signal levels – 0 or 1
      - Could represent any VDD
    - Instantaneous transition times
      - 0s, 0us, 0ns, 0ps



Gate Level Signal Diagrams

- Circuits are evaluated from input to output when creating signal diagrams



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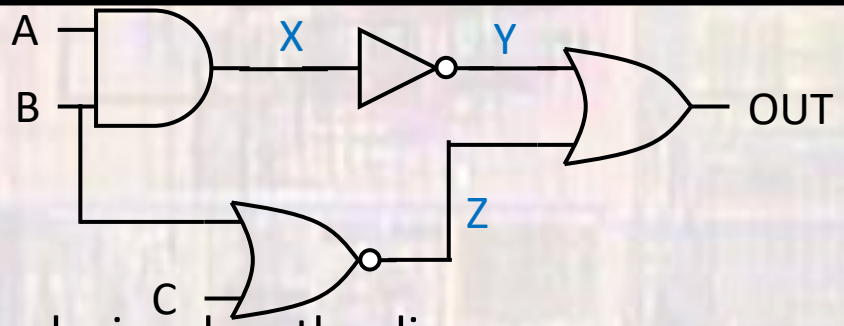
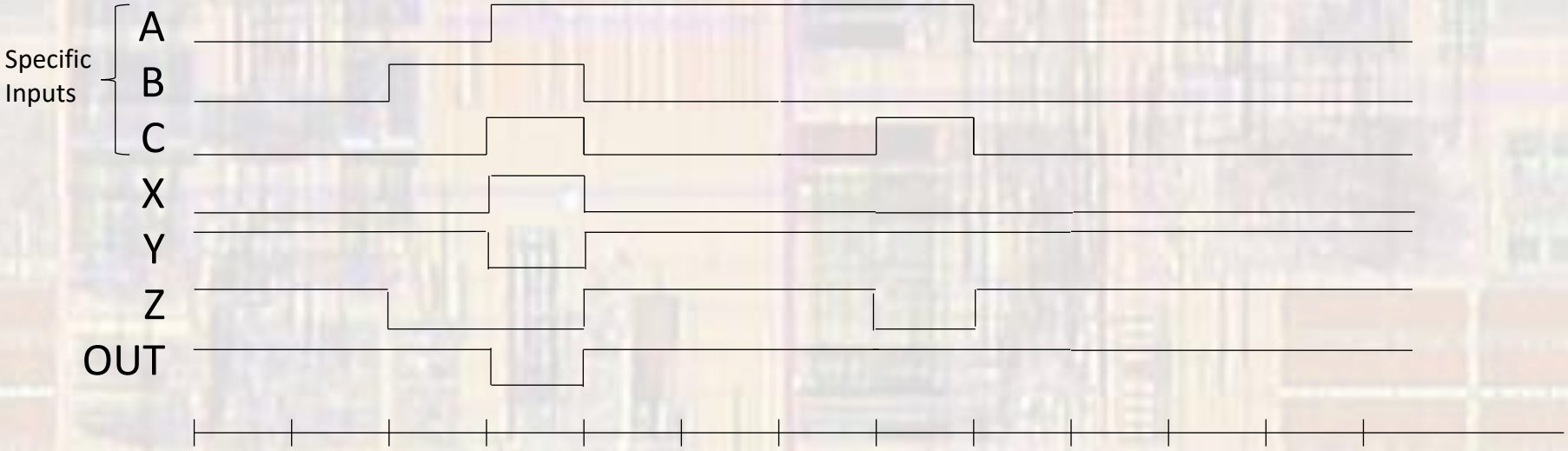


- Signal Diagram Creation
  - Process
    1. Label all intermediate nodes
    2. Create a horizontal section for each signal on the diagram
    3. Create a time scale at the bottom of the diagram
    4. Fill in the input signals
    5. Fill in each intermediate signal until the output signal is complete



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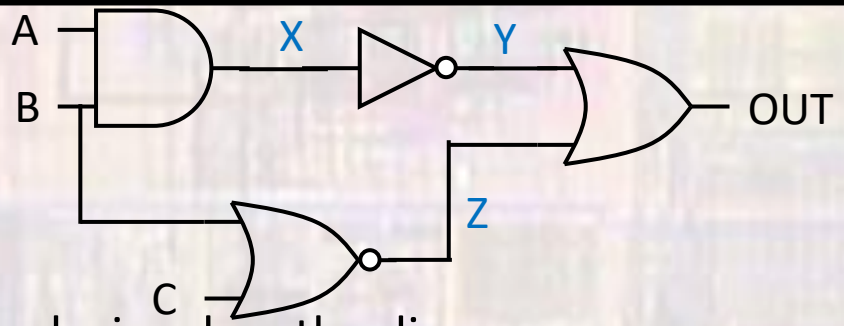

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